

# A Fully Integrated Ku-band PLL in SiGe:C for VSAT Applications

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**Abstract** — Progress with silicon and silicon germanium based BiCMOS technologies over the past few years has been very impressive. Enabling the implementation of traditional microwave applications in silicon.

As an example we present a fully integrated Ku band Phase Locked Loop (PLL) for 13.05 GHz. In this paper we analyse system choices and present measured results of an Integrated RF-PLL in Qubic4X technology [4]. The application is a Ku band Linear Block Up Converter for VSAT systems. The system requires an extremely low phase noise carrier at 13.05 GHz generated from a 10 MHz reference. We will demonstrate overall system performance with a 2 PLL based solution. The first PLL uses a Xtal based VCO and converts this frequency to 204 MHz. The second PLL, subject of this work, converts the 204 MHz to 13.05 GHz. Measurements are performed on a device in a HVQFN24 package, on a 20 mil RO4003 board.

**Index Terms** — Signal generators, Frequency synthesizers, Satellite communication

## I. INTRODUCTION

During the last years we have seen a breakthrough in SiGe:C BiCMOS IC technologies. State-of-the-art BiCMOS [4],[5] have transit frequencies well above 200 GHz. Until recently this could only be achieved with GaAs based processes. Therefore it is now possible to implement traditional microwave applications in silicon. The benefits of implementation in silicon are, next to the much lower cost, the possibility to integrate more functions, because these silicon processes have a very broad range of components available, ranging from digital blocks in CMOS to varactors and many different types of resistors. Examples of circuits that have been realised in this technology can be found in references [10]...[14].

One of the potential high-volume microwave applications is two-way satellite communication. An example of such a system which is already operational is the so-called Very Small Aperture Terminal (VSAT) system. A VSAT is a two-way satellite ground station with a dish antenna diameter in the range of 1.2 to 3 m. VSATs access satellites in geosynchronous orbit to relay data from small remote earth stations (terminals) to other terminals or master earth stations, also called "hubs". The network is depicted in Fig. 1. VSATs are most commonly used to transmit narrowband data (e.g. point of sale

transactions such as credit card), or broadband data up to 4 Mb/s for the provision of Satellite Internet access to remote locations, VoIP or video [1]. Both Time Division Multiple Access and Frequency Division Multiple Access techniques are used to share the satellite bandwidth over the terminals [2]. A VSAT consists of three main subsystems, namely the dish antenna, the outdoor unit (for frequency translation between RF and IF) and the indoor unit (processing the signals between the outdoor unit and the indoor network). The outdoor unit consists of an uplink/downlink separator which is typically a microwave component isolating the downlink from the uplink signals. Furthermore it includes a Low Noise Block (LNB) for receiving the downlink signals and a Block Up Converter (BUC).

In this article we discuss the Local Oscillator (LO) generator for a linear BUC. 'Linear' means the IF to RF conversion is done by mixing with an LO signal. The linear BUC for Ku band uses either 13.05 GHz (for standard range) or 12.8 GHz (for extended range) as LO frequency. To enable precise frequency and time multiplexing the downlink signal provides an accurate frequency reference of 10 MHz. The indoor unit frequency multiplexes this with the uplink IF signal. The LO signal in the BUC needs to be frequency locked to this reference. The specifications are summarized in Table 1.

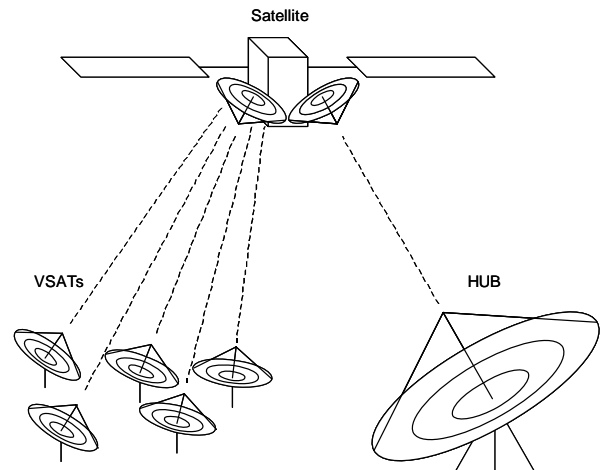


Fig. 1. VSAT Network

TABLE I  
BUC LO GENERATOR SPECIFICATION

Parameter	Conditions	MIN	MAX	UNIT
Temperature		-40	85	° C
Supply voltage		3.0	3.6	V
Supply current			200	mA
Phase noise	Offset freq.			
	100		-55	dBc/Hz
	1k		-72	dBc/Hz
	10k		-82	dBc/Hz
	100k		-92	dBc/Hz
Spurious			-70	dBc
Output power		-7	-3	dBm

## II. LO SUB SYSTEM DESIGN CONSIDERATIONS

The LO generator we designed is a cascade of two PLLs, a clean-up PLL and an RF PLL as shown in Fig. 2. To determine the intermediate frequency between both PLLs, the phase noise requirement must be considered. The RF PLL is realized in a 130 GHz fT SiGe:C process [4]. Free-running VCO phase noise performance of -87 dBc/Hz at 100 kHz offset frequency have been reported in a similar technology [6]. This is clearly not sufficient to meet our requirement of -92 dBc/Hz at 100 kHz. Therefore we use the phase-noise characteristic of a PLL. For offset frequencies below the loop bandwidth (in-band), the phase-noise is determined by the Phase-Frequency Detector (PFD) and the division ratio of the divider. For offset frequencies above the loop bandwidth, the phase-noise is follows the VCO characteristic. In our design the phase noise below 100 kHz is fully determined by the PFD and divider.

In order to determine the division ratio and reference frequency for the RF PLL, we can use the following relation between the in-band phase noise  $L(f)$  versus the PFD Figure of Merit (FOM), division ratio  $N$  and the reference frequency  $f_{ref}$  [7]:

$$L(f) = FOM \left[ \frac{dBc}{Hz^2} \right] + 20 \log_{10} N + 10 \log_{10} f_{ref} \left[ \frac{dBc}{Hz} \right]$$

The FOM reported in this technology is -222 dBc/Hz<sup>2</sup> [6], resulting in an in-band phase-noise floor of -108 dBc/Hz for a division ratio  $N=16$  and reference frequency 816 MHz. This value increases with 3 dB when the division ratio doubles.

We have chosen a division ratio of  $N=64$  with a 204 MHz reference, resulting in an in-band noise floor of -102 dBc/Hz. This will give enough margin over process, voltage and temperature variations as well as an acceptable level of complexity for the clean-up PLL. The clean-up PLL has two functions 1) frequency conversion from 10 MHz to 204 MHz; 2) removal of unwanted phase noise of the 10 MHz reference to the BUC. This is achieved by using a narrow loop bandwidth for the clean-up PLL. The phase noise of the 204 MHz signal should be small compared to the input phase noise of the RF PLL. The input phase noise is now equal to the output phase-noise power divided by  $N^2$ , so  $-102 - 20 \log_{10}(64) = -138$  dBc/Hz. Commercially available VCXOs can meet this requirement [8]. The synthesizer of the clean-up PLL can be implemented as an Integer-N PLL, e.g. a CPLD [3]. For 13.05 GHz we use a reference division ratio of  $N_{ref}=64$ , resulting in a comparison frequency of 156.25 kHz and main division ratio of  $N_{main}=1305$ . Note that in the 12.8 GHz output case, the reference frequency should be set to 200 MHz. Other values for the 12.8 GHz case can be found in Fig. 2.

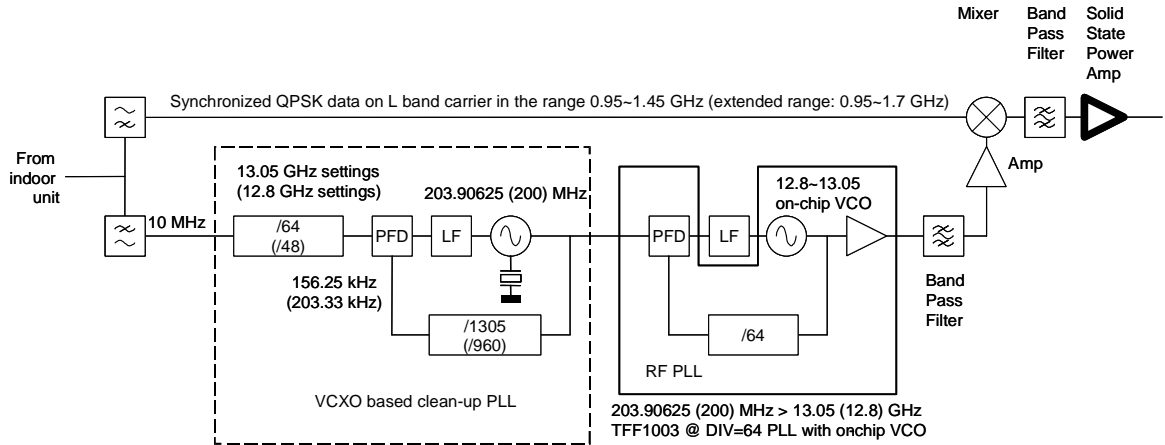


Fig. 2. VSAT Network Complete LO generator for linear Block Up Converter. The values indicated are for the 13.05 GHz output frequency (values for the extended range with 12.8 GHz LO frequency are between brackets)

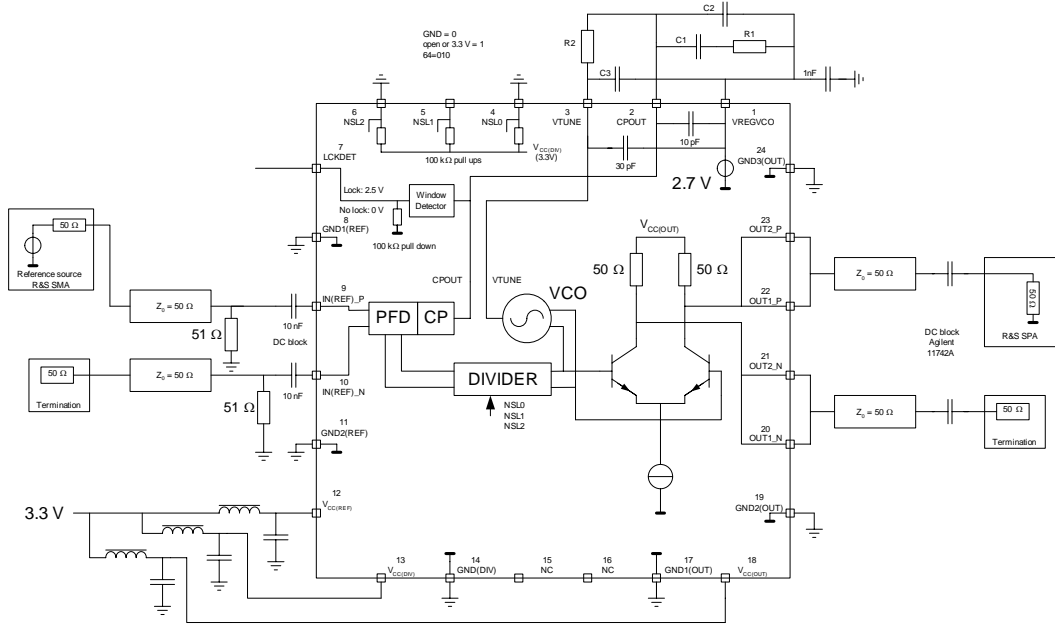


Fig. 3. Detailed block diagram of LO generator and the setup as measured.

## II. IMPLEMENTATION OF THE RF PLL

For the verification of the estimated performance of the complete LO generator, a design was made of a fully integrated RF PLL in a standard SiGe:C BiCMOS technology. The block diagram of the RF PLL is shown in Fig. 3. The VCO has a guaranteed tuning range from 12.8 to 13.05 GHz. The input and output signals are differential. The divider can be set to  $N=16, 32, 64, 128, 256$ . The device has a lock detect output. The assignment of the pins has been done for optimal performance, three voltage domains are used to separate the blocks on the IC. Two pins for each output (OUT\_P and OUT\_N) have been reserved to match to a typical linewidth of a 50 Ohm microstrip line on a Rogers 4003 20 mil board. In our case we used a linewidth of 1.1 mm. Ground pins have been placed next to the reference input and the output. The supply pins are all on the same side of the IC to minimize crossings in the application. The package used for the RF PLL is a standard HVQFN24 (SOT616-1) that uses low-cost wirebonding assembly.

## II. MEASUREMENT RESULTS

The measurements were using the divider setting of  $N=64$ . Fully packaged devices were tested at various operating conditions. We used a temperature range between  $-40^\circ\text{C}$  and  $+85^\circ\text{C}$  and supply voltage range from 3.0 to 3.6V. Fig. 4 shows the measured phase

noise density for a 13.05 GHz carrier. The measured phase noise is  $-94\text{ dBc/Hz @1kHz}$ ,  $-102\text{ dBc/Hz @10kHz}$  and  $-100\text{ dBc/Hz @100kHz}$  over all operating conditions. These values are well below the required levels as listed in table 1. The spurious due to reference signal is shown in Fig. 5, meeting the required level of  $-70\text{ dBc}$ . The measured output power over the tuning range versus temperature is shown in Fig 6. This meets also the required range of  $-3$  to  $-7\text{ dBm}$ . The worst-case measured current consumption is below 104 mA.

## II. CONCLUSIONS

Fully integrated RF PLL functionality in nowadays standard SiGe:C technology is demonstrated on the basis of a LO generator for VSAT systems. The RF-PLL, in the presented system architecture, converts the output of a commercially available VCXO from 204 MHz up to the required 13.05 GHz. Thereby achieving phase noise levels close to  $-100\text{ dBc/Hz}$  for offset frequencies from 5 kHz onwards over all operating conditions. Which is far below the system requirements of  $-92\text{ dBc/Hz}$ . Feasibility of Si technologies for LO generation at microwave frequencies is proven.

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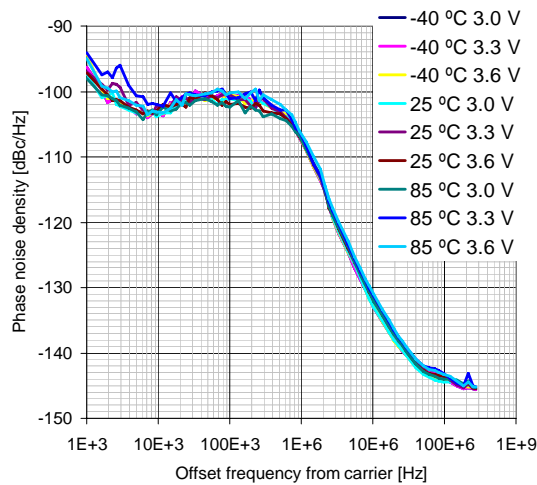


Fig. 4. Phase noise density (13.05 GHz carrier). Performance better than  $-100$  dBc/Hz for offset frequencies  $> 5$  kHz

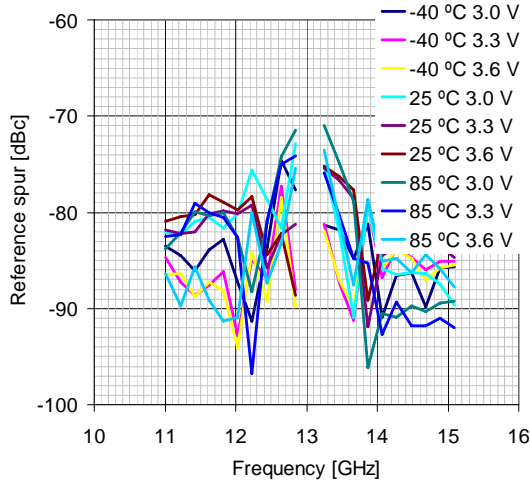


Fig. 5. Spurious from 204 MHz reference (13.05 GHz carrier). Performance better than  $-71$  dBc.

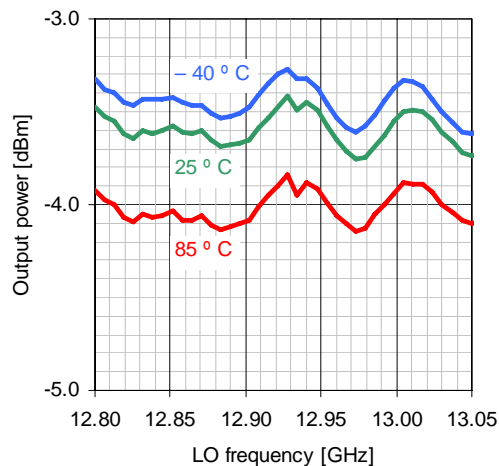


Fig. 6. Output power (13.05 GHz carrier). Output power stays between  $-3.2$  and  $-4.2$  over temperature and frequency.

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