

# AN\_BLL6H1214-500

## BLL6H1214-500 LDMOS Transistor Model

Rev. 01 — 18-05-2009

Application note

### Document information

Info	Content
<b>Keywords</b>	BLL6H1214_500, BLL6H1214_500_ LDMOS, model
<b>Abstract</b>	This document describes the BLL6H1214_500 LDMOS transistor model including its installation.

## Revision history

Rev	D	Description
01	20090518	Initial revision

## Contact information

For additional information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Table of contents

1. Introduction..... 4

2. Model Description ..... 4

3. Model Parameters..... 5

4. Parameter extraction procedure ..... 6

5. Installation Instructions ..... 7

5.1 Case 1: No RFLDMOS model library installed..... 7

5.2 Case 2: Old version of the RFLDMOS model library installed ..... 7

5.3 Case 3: Updated version of the RFLDMOS model library installed ... 7

6. Legal Information ..... 9

6.1 Definitions..... 9

6.2 Disclaimers ..... 9

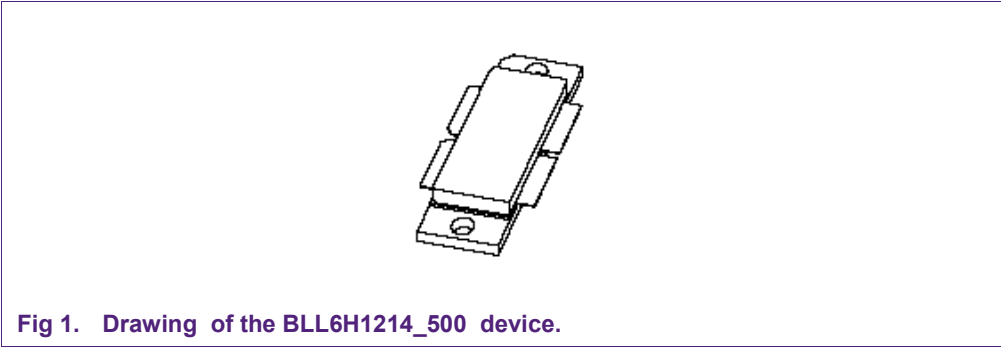
6.3 Patents ..... 9

6.4 Trademarks ..... 9

## 1. Introduction

The purpose of this document is to provide the customer with a comprehensive description of the BLL6H1214\_500LDMOS transistor model, extraction procedure and installation procedure.

BLL6H1214\_500 is a 500 W RF power transistor (see [Fig 1](#)). The device has been optimized for applications in the 1200—1400 MHz frequency band. For more information about the device performance, see the Data Sheet.



## 2. Model Description

[Table 1](#) summarizes the model information.

**Table 1. Summary of model information**

Device name	BLL6H1214_500
Model name	NXP_ BLL6H1214_500
Model version	0.1
Simulator	ADS 2006A
Library version	RFLDMOS 10.0

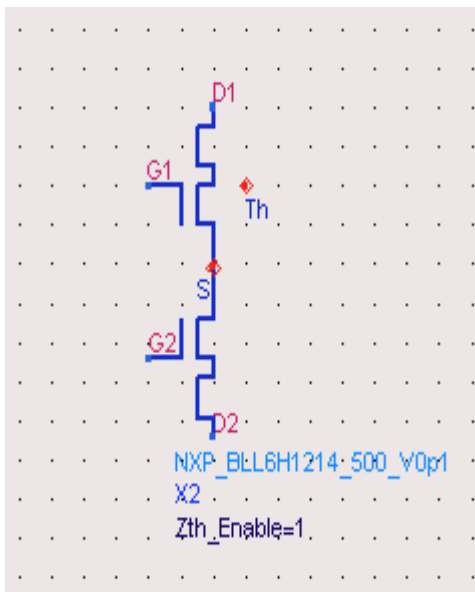
The electrical behavior of the transistor die is described by a scalable, physics based, fully electro-thermal RFLDMOS model<sup>1</sup>. The model scales with the number of cells, the length of the gate fingers and with the finger-to-finger pitch. The interconnecting structures on the die are modeled by the means of EM simulations and lumped.

1. See: M.B. Willemsen\*, R. van Langevelde\*\* and D.B.M. Klaassen, “*High-Voltage LDMOS Compact Modelling*”, NIST-Nanotech 2006, Vol. 3 2006, pgg. 714 – 719.

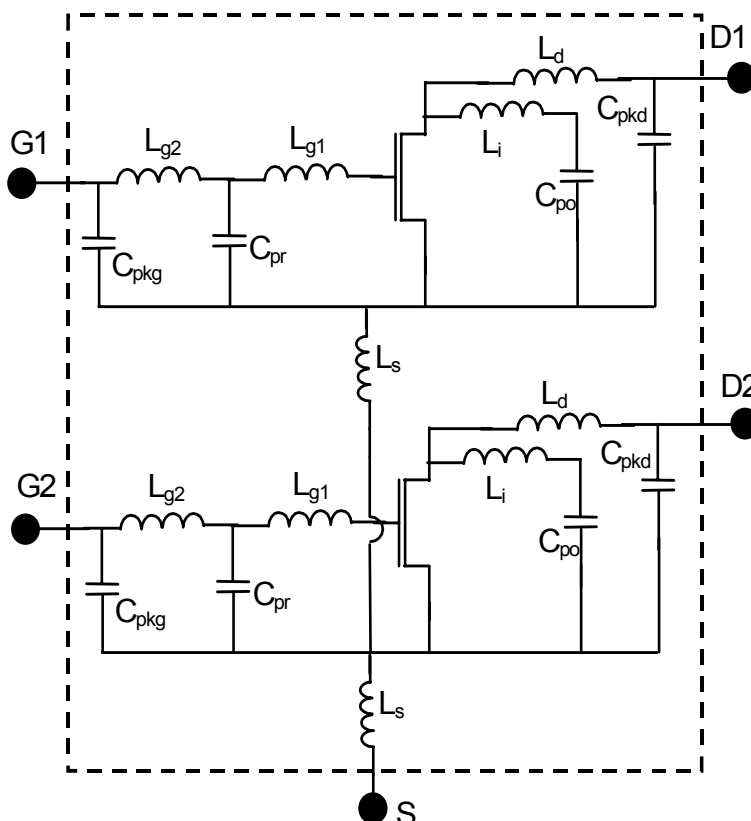
Equivalent circuits. Lumped elements and bondwire component models are used to model the various package elements<sup>2</sup>.

### 3. Model Parameters

The ADS symbol for the BLL6H1214\_500 device is shown in Fig 2.



**Fig 2. ADS symbol of the BLL6H1214\_500 device model.**



**Fig 3. Schematic of the package model as in Fig 2.**

The simulation temperature is controlled by the “Tamb” temperature parameter of the ADS “Option” block.

The “Th” node is thermal node of the device and must be connected to the ground either directly or through a RC-parallel network which may be used to describe an additional or alternative external thermal network<sup>3</sup>.

2. These components might not be suitable to support time-domain simulations such as transient simulations or transient-assisted HB simulations. Please contact NXP Semiconductors if this constitutes a problem.
3. Failing to connect the “Th” node to the ground either directly or through a RC-parallel network will cause the non-convergence of simulations.

The “Zth\_Enable” parameter allows enabling or disabling the default thermal network of the device. This parameter can be used in combination with an external thermal network to reproduce the following situations:

1. Zth\_Enable set to 0, Th node connected to ground directly: Isothermal simulations.
2. Zth\_Enable set to 0, Th node connected to ground through a RC-parallel network: ET simulations with the external RC-parallel as thermal network.
3. Zth\_Enable set to 1, Th node connected to ground directly: ET simulations with the default device thermal network.
4. Zth\_Enable set to 1, Th node connected to ground through a RC-parallel network: ET simulations with the series of the external RC-parallel and the device default as thermal network.

The parameter Cpr\_Spread, allow controlling the spread of the values of the bond-wire inductances and matching capacitances. In practice, the parameters set the ratio between the actual and nominal values of each element<sup>4</sup>. By default, these parameters are set to 1.

The expected statistical distributions of the spreading of the bond-wire inductances and matching capacitances are available and can be provided by NXP on special request

## 4. Parameter extraction procedure

The model parameters of each section were extracted with the following procedure:

- i. Extraction of the parameters of the active die model
  - a. The DC characteristics were measured in wide bias and temperature ranges ( $V_{gs}$  up to 15V,  $V_{ds}$  up to 30V, T up to 125 °C).
  - b. The s-parameter were measured in a wide frequency band
  - c. Dedicated structures were used for the de-embedding of the parasitics due to metal structures and interconnects from the s-parameter data.
  - d. A semi-automated procedure implemented with the Agilent's IC-CAP program was used to extract the model parameters
- ii. Extraction of the parameters of the package model
  - a. The values of the matching capacitances are obtained from design information
  - b. The value of the package parasitic capacitance is measured with a low-frequency CV meter
  - c. The starting values of the bondwire models are obtained from design information.

5. For instance, by setting  $L_{g1\_spread}$  to 0.95, the actual value of the  $L_{g1}$  inductance becomes 95% its nominal value.

## 5. Installation Instructions

---

In order to run properly, the Design Kit requires the latest version of the NXP RFLDMOS model library to be installed (see [Table 1](#) for version information). The RFLDMOS model library provides the definitions of the primitive submodels employed by the main device model. The installation procedure is described for three possible cases.

### 5.1 Case 1: No RFLDMOS model library installed

- i. Close all ADS schematics
- ii. In the main window of ADS, select "Design Kit -----> Install Design Kits....."
- iii. Install the NXP RFLDMOS model library
- iv. Exit and restart ADS
- v. In the main window of ADS, select "Design Kit -----> Install Design Kits....."
- vi. Install the model Design Kit
- vii. Exit and restart ADS
- viii. Now the model will function properly

### 5.2 Case 2: Old version of the RFLDMOS model library installed

- i. Close all schematics
- ii. In the main window of ADS, select "Design Kit -----> Setup Design Kits....."
- iii. REMOVE the older version of the RFLDMOS model library (NOT just DISABLE)
- iv. Apply the changes
- v. Exit and restart ADS
- vi. In the main window of ADS, select "Design Kit -----> Install Design Kits....."
- vii. Install the RFLDMOS model library
- viii. Exit and restart ADS
- ix. In the main window of ADS, select "Design Kit -----> Install Design Kits....."
- x. Install the model Design Kit
- xi. Exit and restart ADS
- xii. Now the model will function properly

### 5.3 Case 3: Updated version of the RFLDMOS model library installed

- i. Close all schematics
- ii. In the main window of ADS, select "Design Kit -----> Install Design Kits....."
- iii. Install the Design Kit of the model
- iv. Exit and restart ADS
- v. Now the model will function properly

**NOTE**: failing to have the proper version of the RFLDMOS model library installed will result in an error message during the simulations.

The properties of the layers and the values of the components are listed in the table below.



## 6. Legal Information

### 6.1 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

### 6.2 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is for the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

### 6.3 Patents

Notice is herewith given that the subject device uses one or more patents and that each of these patents may have corresponding patents in several jurisdictions.

### 6.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are property of their respective owners.

**ADS** — is a trademark of Agilent Technologies

**Momentum** — is a trademark of Agilent Technologies

**IC-CAP** — is a trademark of Agilent Technologies

