

# AN\_BLF6G27LS-135

## BLF6G27-135 LDMOS Transistor Model

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Application note

### Document information

Info	Content
<b>Keywords</b>	BLF6G27-135, BLF6G27(LS)-135 LDMOS, model
<b>Abstract</b>	This document describes the BLF6G27LS-135 LDMOS transistor model including its installation, usage and verification.

Revision history

Rev	D	Description
01	20070813	Initial revision

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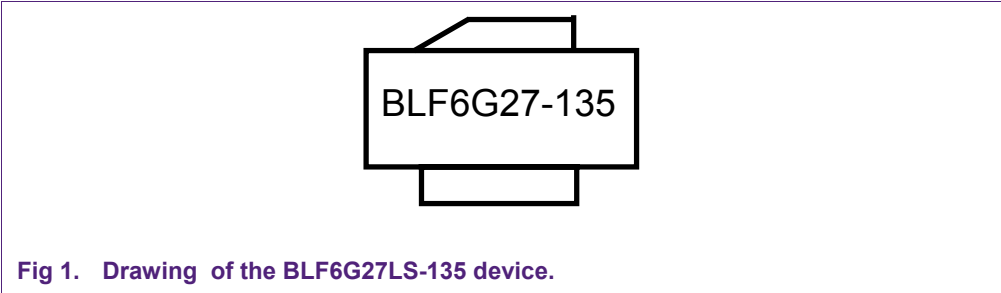
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1. Introduction

The purpose of this document is to provide the customer with a comprehensive description of the BLF6G27LS-135LDMOS transistor model, extraction procedure, installation procedure, verification, limitations and application.

The BLF6G27LS-135 is a 135W RF power transistor (see [Fig 1](#)). The device has been optimized for applications in the 2.5—2.7 GHz frequency band. For more information about the device performance, see the Data Sheet.



2. Model Description

[Table 1](#) summarizes the model information.

**Table 1. Summary of model information**

Device name	BLF6G27-135, BLF6G27LS-135
Model name	NXP_ BLF6G27LS-135
Model version	1.1
Simulator	ADS 2005A, ADS2006A
Library version	RFLDMOS 8.01

The electrical behavior of the transistor die is described by a scalable, physics based, fully electro-thermal RFLDMOS model<sup>1</sup>. The model scales with the number of cells, the length of the gate fingers and with the finger-to-finger pitch. The interconnecting structures on the die are modeled by the means of EM simulations and lumped.

1. Due to software issues, at this moment there is no compatibility with other releases of ADS. In case this constitutes a problem, please contact NXP Semiconductors.

2. See: M.B. Willemsen\*, R. van Langevelde\*\* and D.B.M. Klaassen, “*High-Voltage LDMOS Compact Modelling*”, NIST-Nanotech 2006, Vol. 3 2006, pgg. 714 – 719.

Equivalent circuits. Lumped element components are used to model the matching capacitors, package parasitic capacitance and bond-wire inductances<sup>2</sup>.

### 3. Model Parameters

The ADS symbol for the BLF6G27-135 device is shown in Fig 2.

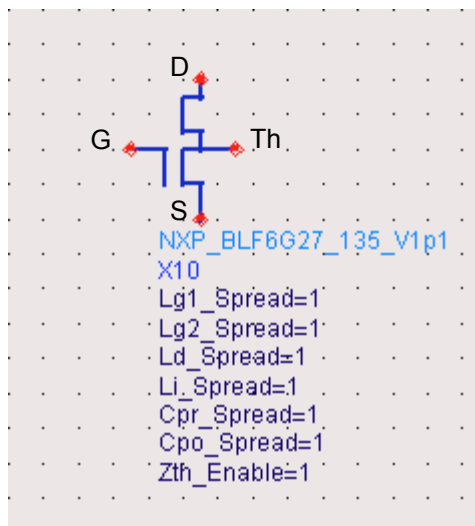


Fig 2. ADS symbol of the BLF6G27LS-135 device model.

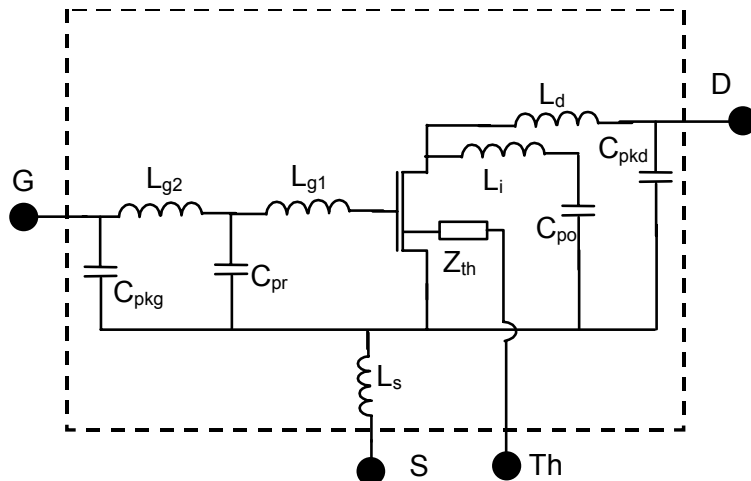


Fig 3. Schematic of the package model as in Fig 2.

The simulation temperature is controlled by the “Tamb” temperature parameter of the ADS “Option” block.

The “Th” node is thermal node of the device and must be connected to the ground either directly or through a RC-parallel network which may be used to describe an additional or alternative external thermal network<sup>3</sup>.

The “Zth\_Enable” parameter allows enabling or disabling the default thermal network of the device. This parameter can be used in combination with an external thermal network to reproduce the following situations:

1. Zth\_Enable set to 0, Th node connected to ground directly: Isothermal simulations.
2. Zth\_Enable set to 0, Th node connected to ground through a RC-parallel network: ET simulations with the external RC-parallel as thermal network.
3. Zth\_Enable set to 1, Th node connected to ground directly: ET simulations with the default device thermal network.

3. The lumped components models employed are not suitable to support time-domain simulations such as transient simulations or transient-assisted HB simulations. Please contact NXP Semiconductors if this constitutes a problem.
4. Failing to connect the “Th” node to the ground either directly or through a RC-parallel network will cause the non-convergence of simulations.

4. Zth\_Enable set to 1, Th node connected to ground through a RC-parallel network: ET simulations with the series of the external RC-parallel and the device default as thermal network.

The parameters  $L_{g1\_Spread}$ ,  $L_{g2\_Spread}$ , etc. allow controlling the spread of the values of the bond-wire inductances and matching capacitances. In practice, the parameters set the ratio between the actual and nominal values of each element<sup>4</sup>. By default, these parameters are set to 1.

The expected statistical distributions of the spreading of the bond-wire inductances and matching capacitances are available and can be provided by NXP on special request

## 4. Parameter extraction procedure

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The model parameters of each section were extracted with the following procedure:

- i. Extraction of the parameters of the active die model
  - a. The DC characteristics were measured in wide bias and temperature ranges ( $V_{gs}$  up to 15V,  $V_{ds}$  up to 30V, T up to 125 °C).
  - b. The s-parameter were measured in a wide frequency band
  - c. Dedicated structures were used for the de-embedding of the parasitics due to metal structures and interconnects from the s-parameter data.
  - d. A semi-automated procedure implemented with the Agilent's IC-CAP program was used to extract the model parameters
- ii. Extraction of the parameters of the package model
  - a. The values of the matching capacitances are obtained from design information
  - b. The value of the package parasitic capacitance is measured with a low-frequency CV meter
  - c. The starting values of the bond-wire inductances are obtained from design information.
  - d. The device S-parameters are measured using both an unmatched test fixture<sup>5</sup> and the application circuit.
  - e. The inductance values are then optimized by fitting the S-parameters data. The package parasitic source inductance is also optimized.

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5. For instance, by setting  $L_{g1\_spread}$  to 0.95, the actual value of the  $L_{g1}$  inductance becomes 95% its nominal value.

6. This test fixture is composed by a simple 50Ω transmission line and, therefore, provides 50Ω loadings at the input and output of the device.

## 5. Installation Instructions

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In order to run properly, the Design Kit requires the latest version of the NXP RFLDMOS model library to be installed (see [Table 1](#) for version information). The RFLDMOS model library provides the definitions of the primitive submodels employed by the main device model. The installation procedure is described for three possible cases.

### 5.1 Case 1: No RFLDMOS model library installed

- i. Close all ADS schematics
- ii. In the main window of ADS, select "Design Kit -----> Install Design Kits....."
- iii. Install the NXP RFLDMOS model library
- iv. Exit and restart ADS
- v. In the main window of ADS, select "Design Kit -----> Install Design Kits....."
- vi. Install the model Design Kit
- vii. Exit and restart ADS
- viii. Now the model will function properly

### 5.2 Case 2: Old version of the RFLDMOS model library installed

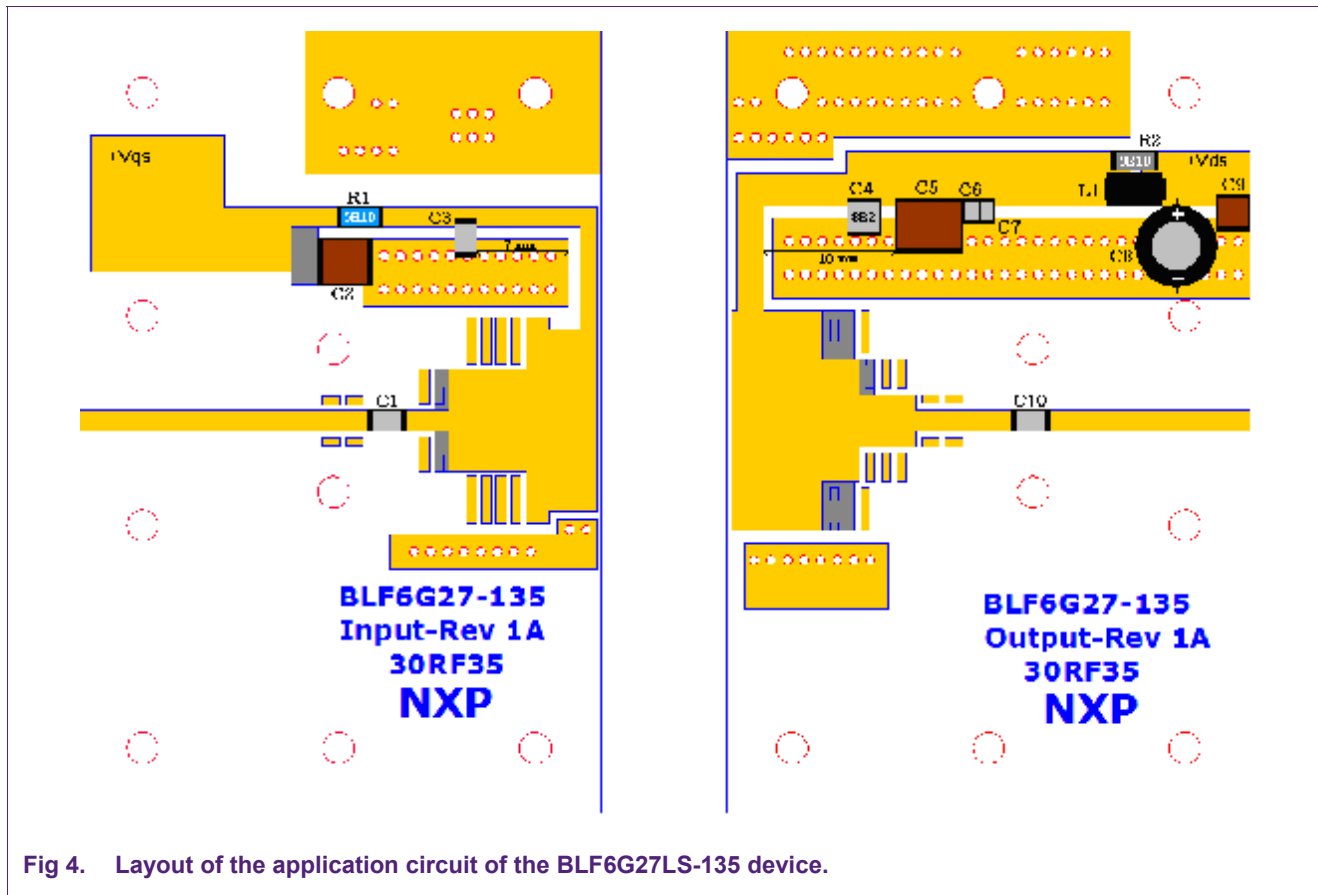
- i. Close all schematics
- ii. In the main window of ADS, select "Design Kit -----> Setup Design Kits....."
- iii. REMOVE the older version of the RFLDMOS model library (NOT just DISABLE)
- iv. Apply the changes
- v. Exit and restart ADS
- vi. In the main window of ADS, select "Design Kit -----> Install Design Kits....."
- vii. Install the RFLDMOS model library
- viii. Exit and restart ADS
- ix. In the main window of ADS, select "Design Kit -----> Install Design Kits....."
- x. Install the model Design Kit
- xi. Exit and restart ADS
- xii. Now the model will function properly

### 5.3 Case 3: Updated version of the RFLDMOS model library installed

- i. Close all schematics
- ii. In the main window of ADS, select "Design Kit -----> Install Design Kits....."
- iii. Install the Design Kit of the model
- iv. Exit and restart ADS
- v. Now the model will function properly

**NOTE:** failing to have the proper version of the RFLDMOS model library installed will result in an error message during the simulations.

The layout drawing of the modeled application circuit is shown in Fig 4<sup>6</sup>.



The properties of the layers and the values of the components are listed in the table below.

**Table 2. Characteristics of the layers of the application circuit board**

Layer	Material	Thickness
Substrate	Rodgers ( $\epsilon_r = 3.5$ )	0.76 mm
Conductor	Copper	35 $\mu\text{m}$

<sup>6</sup> The DC bias circuit has not been fully included in the actual model of the Test Board.



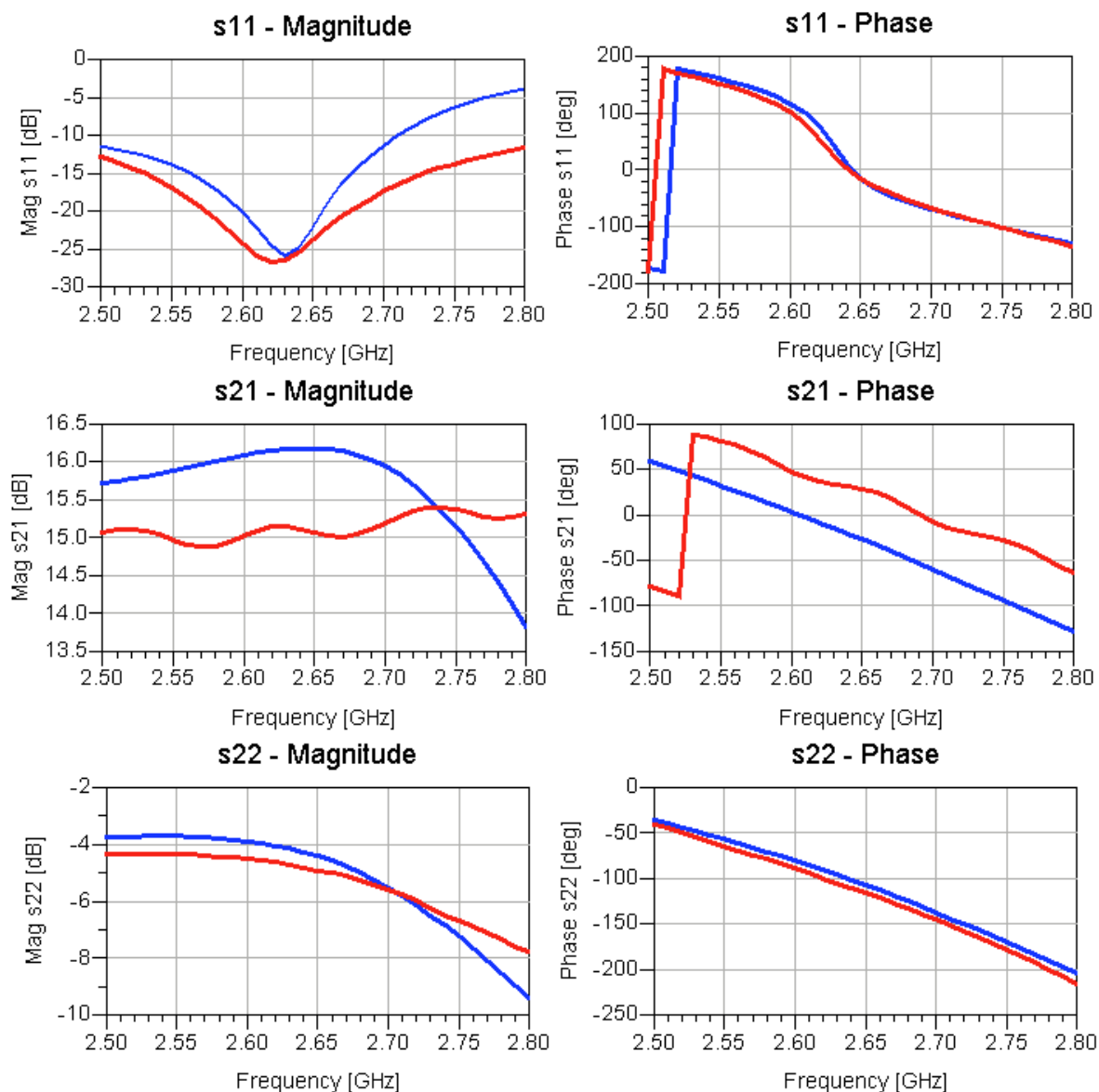
Bill Of Materials			
Description	Component	Type	Value
Base plate			
Input pcb BLF6G27(LS)-135		Taconic RF35	0.76mm / 40x60mm
		double sided	$\epsilon_r = 3.5 / 1 \text{ oz.}$
Output pcb BLF6G27(LS)-135		Taconic RF35	0.76mm / 40x60mm
		double sided	$\epsilon_r = 3.5 / 1 \text{ oz.}$
21x Bolt M2			M2 x 5mm
21x Washer M2			M2
Position block SOT502			
Multilayer ceramic chip capacitor	C1,C3,C4,C10	ATC 100B	8.2pF
Multilayer ceramic chip capacitor	C2	C4532X7R1H475M	4.7uF/50V
Multilayer ceramic chip capacitor	C5	C5750X7R1H106M	10uF/50V
Multilayer ceramic chip capacitor	C9	C3225X7R1H155M	1.5uF/50V
Multilayer ceramic chip capacitor	C6,C7	VJ1206Y104KXB	100nF
Electrolytic capacitor	C8		470uF/63V
Resistor	R1	SMD 1206	5.1 ohm
Resistor	R2	SMD 1206	9.1 ohm

## 7. Model Verification

### 7.1 DC Verification

At present, no DC verification data is available.

## 7.2 Small-signal verification



**Fig 5.** Measured (red lines) and simulated (blue lines) magnitudes and phases of the  $s_{11}$ ,  $s_{21}$  and  $s_{22}$  parameters of the BLF6G27LS-135 LDMOS device.

The conditions for the above graphs are:  $I_{dq}=1200$  mA,  $V_{ds}=28$ V.

### 7.3 One Tone Verification

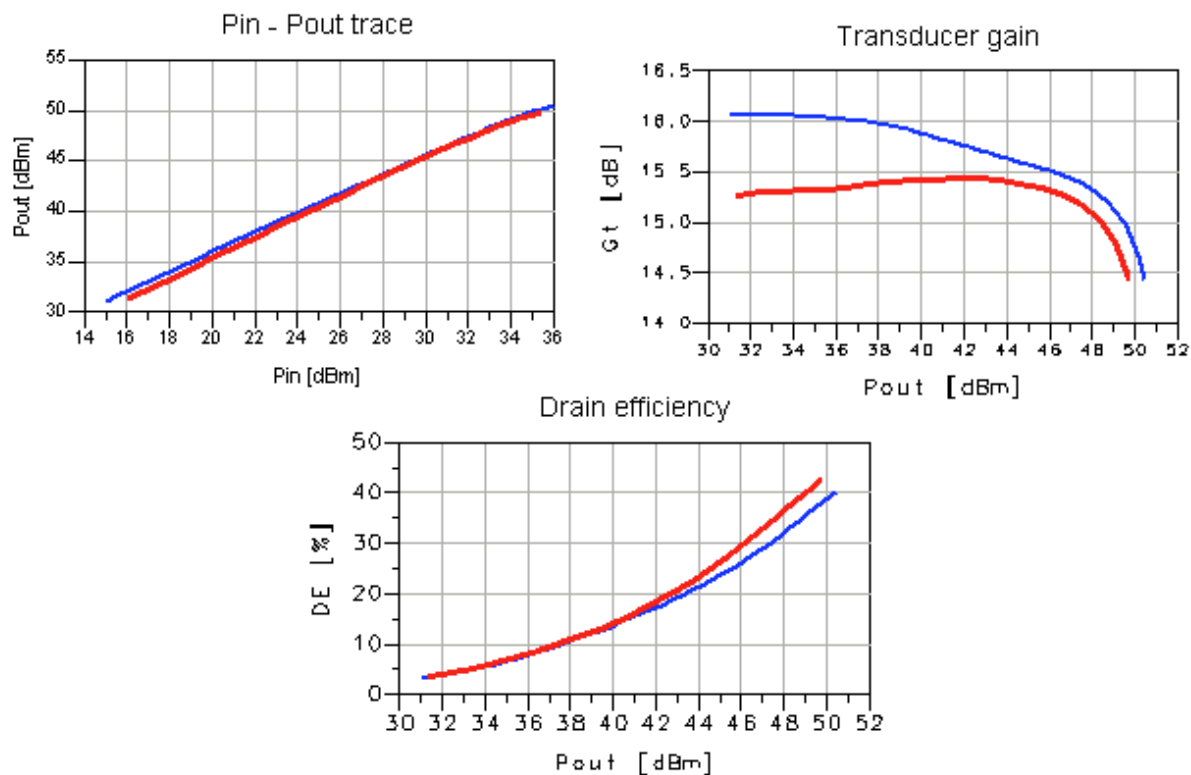


Fig 6. Measured (red lines) and simulated (blue lines) 1-tone large-signal performance of the BLF6G27-135LS LDMOS device.

The conditions for the above graphs are:  $I_{dq}=1200\text{mA}$ ,  $V_{ds}=28\text{V}$ ,  $f=2.6\text{GHz}$ .

## 7.4 Two Tone Verification

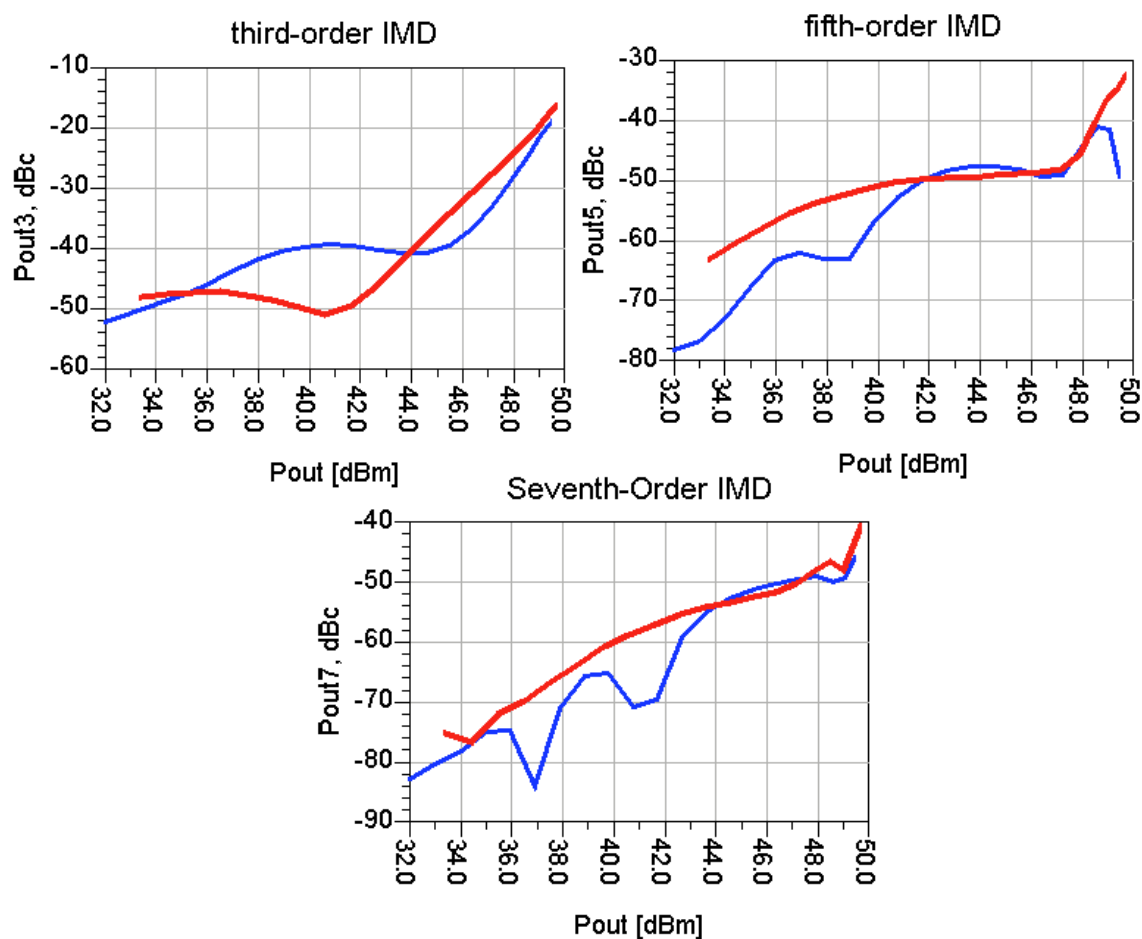


Fig 7. Measured (red lines) and simulated (blue lines) 2-tone large-signal performance of the BLF6G27-135LS LDMOS device.

The conditions for the above graphs are:  $I_{dq}=1200\text{mA}$ ,  $V_{ds}=28\text{V}$ ,  $f=2.6\text{GHz}$ ,  $\Delta f=100\text{ kHz}$ .

## 7.5 Summary of the model performance

- In-band s-parameters well predicted.
- $P_{1db}$  slightly overestimated
- PAE well-predicted
- Trends of IMD3, IMD5 and IMD7 well-predicted

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