

AN_BLF645

BLF645 LDMOS Transistor Model

Rev. 01st — 12-07-2008

Application note

Document information

Info	Content
Keywords	BLF645, BLF645 _ LDMOS, model
Abstract	This document describes the BLF645 _ LDMOS transistor model including its installation.

Revision history

Rev	D	Description
01	20071025	Initial revision

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1. Introduction

The purpose of this document is to provide the customer with a comprehensive description of the BLF645 _ LDMOS transistor model, extraction procedure and installation procedure.

The BLF645 _ LDMOS is a 100W RF power transistor (see [Fig 1](#)). The device has been optimized for applications in the 1.2—1.4 GHz frequency band. For more information about the device performance, see the Data Sheet.

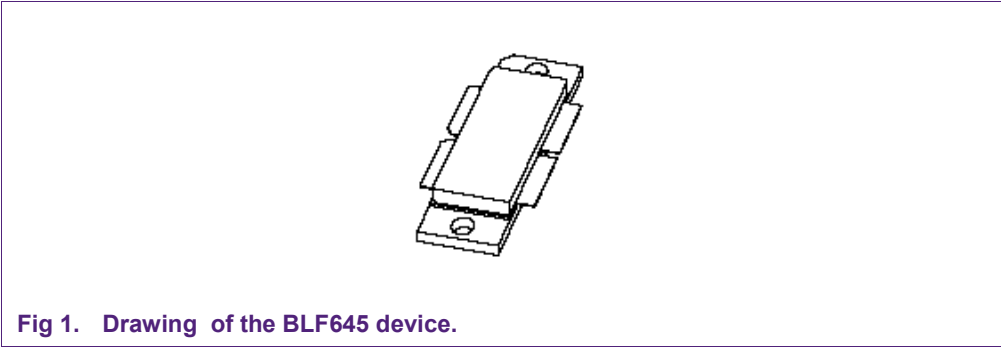


Fig 1. Drawing of the BLF645 device.

2. Model Description

[Table 1](#) summarizes the model information.

Table 1. Summary of model information

Device name	BLF645
Model name	NXP_ BLF645
Model version	0.3sm
Simulator	ADS 2005A, ADS 2006A
Library version	RFLDMOS 10.0

The electrical behavior of the transistor die is described by a scalable, physics based, fully electro-thermal RFLDMOS model¹. The model scales with the number of cells, the length of the gate fingers and with the finger-to-finger pitch. The interconnecting structures on the die are modeled by the means of EM simulations and lumped.

1. See: M.B. Willemsen*, R. van Langevelde** and D.B.M. Klaassen, “*High-Voltage LDMOS Compact Modelling*”, NIST-Nanotech 2006, Vol. 3 2006, pgg. 714 – 719.

Equivalent circuits. Lumped elements and bondwire component models are used to model the various package elements².

3. Model Parameters

The ADS symbol for the BLF645 device is shown in Fig 2.

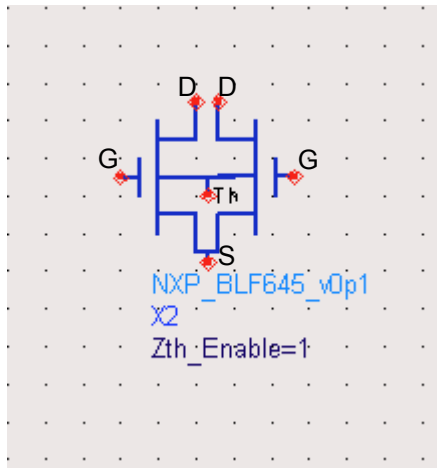


Fig 2. ADS symbol of the BLF645 device model.

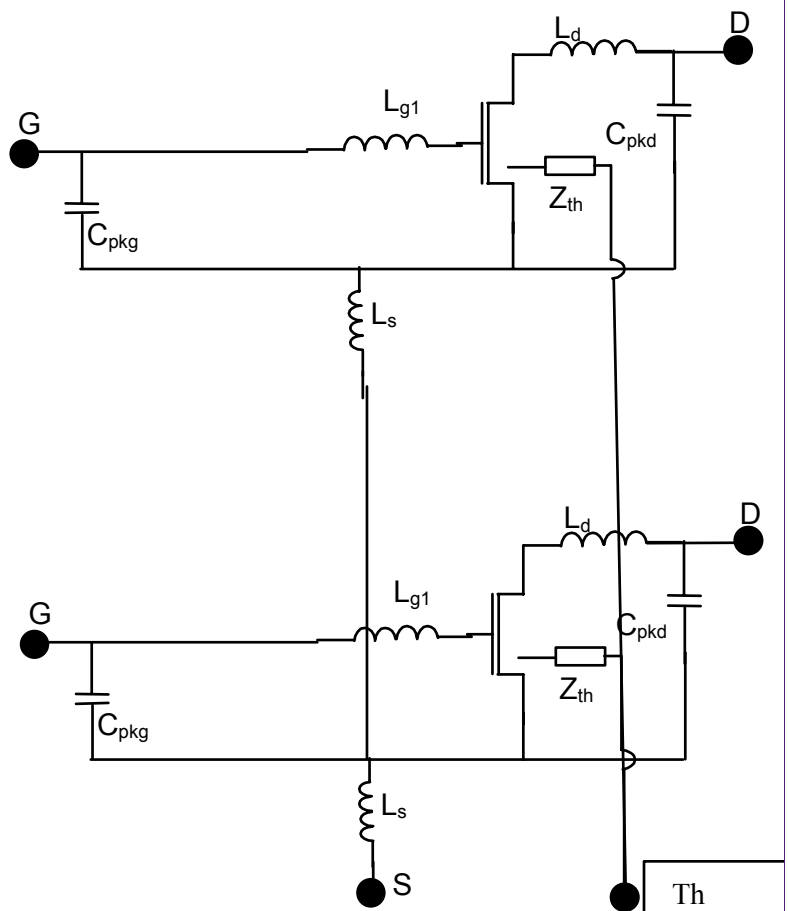


Fig 3. Schematic of the package model as in Fig 2.

The simulation temperature is controlled by the “Tamb” temperature parameter of the ADS “Option” block.

- These components might not be suitable to support time-domain simulations such as transient simulations or transient-assisted HB simulations. Please contact NXP Semiconductors if this constitutes a problem.

The “Th” node is thermal node of the device and must be connected to the ground either directly or through a RC-parallel network which may be used to describe an additional or alternative external thermal network³.

The “Zth_Enable” parameter allows enabling or disabling the default thermal network of the device. This parameter can be used in combination with an external thermal network to reproduce the following situations:

1. Zth_Enable set to 0, Th node connected to ground directly: Isothermal simulations.
2. Zth_Enable set to 0, Th node connected to ground through a RC-parallel network: ET simulations with the external RC-parallel as thermal network.
3. Zth_Enable set to 1, Th node connected to ground directly: ET simulations with the default device thermal network.
4. Zth_Enable set to 1, Th node connected to ground through a RC-parallel network: ET simulations with the series of the external RC-parallel and the device default as thermal network.

The parameter Cpr_Spread. allow controlling the spread of the values of the bond-wire inductances and matching capacitances. In practice, the parameters set the ratio between the actual and nominal values of each element⁴. By default, these parameters are set to 1.

The expected statistical distributions of the spreading of the bond-wire inductances and matching capacitances are available and can be provided by NXP on special request

4. Parameter extraction procedure

The model parameters of each section were extracted with the following procedure:

- i. Extraction of the parameters of the active die model
 - a. The DC characteristics were measured in wide bias and temperature ranges (V_{gs} up to 15V, V_{ds} up to 30V, T up to 125 °C).
 - b. The s-parameter were measured in a wide frequency band
 - c. Dedicated structures were used for the de-embedding of the parasitics due to metal structures and interconnects from the s-parameter data.
 - d. A semi-automated procedure implemented with the Agilent's IC-CAP program was used to extract the model parameters
 - ii. Extraction of the parameters of the package model
 - a. The values of the matching capacitances are obtained from design information
 - b. The value of the package parasitic capacitance is measured with a low-frequency CV meter
 - c. The starting values of the bondwire models are obtained from design information.
-
3. Failing to connect the “Th” node to the ground either directly or through a RC-parallel network will cause the non-convergence of simulations.
 5. For instance, by setting L_{g1_spread} to 0.95, the actual value of the L_{g1} inductance becomes 95% its nominal value.

5. Installation Instructions

In order to run properly, the Design Kit requires the latest version of the NXP RFLDMOS model library to be installed (see [Table 1](#) for version information). The RFLDMOS model library provides the definitions of the primitive submodels employed by the main device model. The installation procedure is described for three possible cases.

5.1 Case 1: No RFLDMOS model library installed

- i. Close all ADS schematics
- ii. In the main window of ADS, select "Design Kit -----> Install Design Kits....."
- iii. Install the NXP RFLDMOS model library
- iv. Exit and restart ADS
- v. In the main window of ADS, select "Design Kit -----> Install Design Kits....."
- vi. Install the model Design Kit
- vii. Exit and restart ADS
- viii. Now the model will function properly

5.2 Case 2: Old version of the RFLDMOS model library installed

- i. Close all schematics
- ii. In the main window of ADS, select "Design Kit -----> Setup Design Kits....."
- iii. REMOVE the older version of the RFLDMOS model library (NOT just DISABLE)
- iv. Apply the changes
- v. Exit and restart ADS
- vi. In the main window of ADS, select "Design Kit -----> Install Design Kits....."
- vii. Install the RFLDMOS model library
- viii. Exit and restart ADS
- ix. In the main window of ADS, select "Design Kit -----> Install Design Kits....."
- x. Install the model Design Kit
- xi. Exit and restart ADS
- xii. Now the model will function properly

5.3 Case 3: Updated version of the RFLDMOS model library installed

- i. Close all schematics
- ii. In the main window of ADS, select "Design Kit -----> Install Design Kits....."

- iii. Install the Design Kit of the model
- iv. Exit and restart ADS
- v. Now the model will function properly

NOTE: failing to have the proper version of the RFLDMOS model library installed will result in an error message during the simulations.

The properties of the layers and the values of the components are listed in the table below.

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Date of release: 12-07-2008

Document order number:

Published in The Netherlands