

# AN\_BLF574

## BLF574 LDMOS Transistor Model

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Application note

### Document information

Info	Content
<b>Keywords</b>	BLF574, BLF574, LDMOS, model
<b>Abstract</b>	This document describes the BLF574 LDMOS transistor model including its installation, usage and verification.

## Revision history

Rev	D	Description
01	20070613	Initial revision

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1. Introduction

The purpose of this document is to provide the customer with a comprehensive description of the BLF574 LDMOS transistor model, extraction procedure, installation procedure, limitations and application.

The BLF574 is a 400W RF (Two tone average) power transistor (see [Fig 1](#)). The device has been optimized for applications in the 225 MHz frequency band. For more information about the device performance, see the Data Sheet.

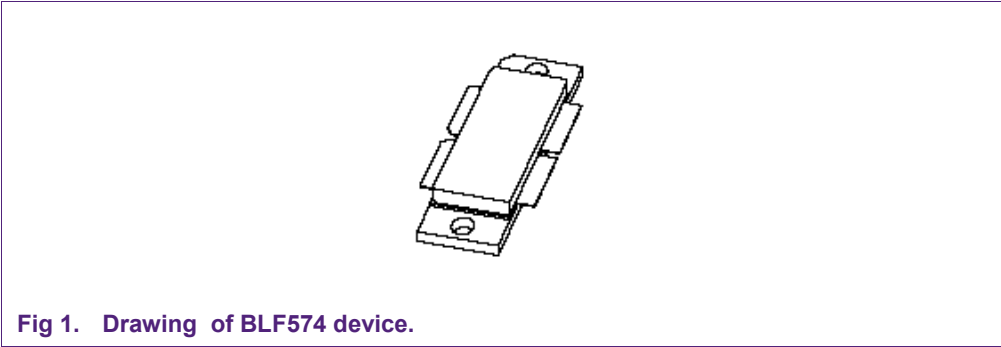


Fig 1. Drawing of BLF574 device.

2. Model Description

[Table 1](#) summarizes the model information.

**Table 1. Summary of model information**

Device name	BLF574, BLF574
Model name	NXP_ BLF574
Model version	0.1
Simulator	ADS 2005A, ADS2006A
Library version	SiMKit 2.4

The electrical behavior of the transistor die is described by a scalable, physics based Sub-Circuit model<sup>1</sup>. This model is based on the Philips standard models MM11 for the channel region and MM31 for the drain extended region. MM11 is a surface potential based MOST model providing a smooth transfer from sub- to super threshold including the sign swap of the temperature coefficient of the drain current. This improves inter-

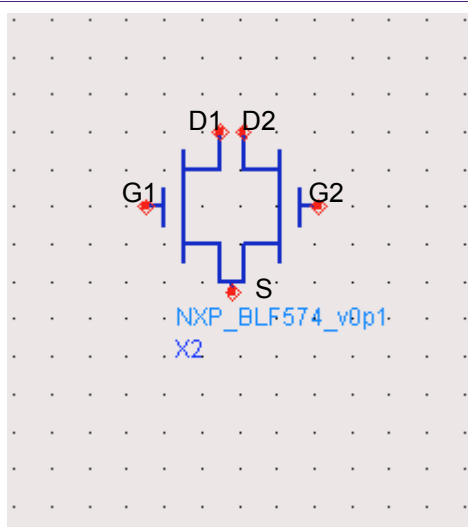
1. See: M.P.J.G. Versleijen, V.J. Bloem, J.A. van Steenwijk, O.I. Yanson, “A new physics based dynamic electro thermal large signal model for RF LDMOS FETs”, IEEE MTT-S 2004 International Microwave Symposium Digest, Volume 1, pgg. 39 – 42.

modulation distortion modeling. In addition, parasitic resistances and capacitances have been included to model the interconnect lines on the die. The model scales with the number of cells and the length of the gate fingers. Temperature scaling of the model is a static one and is based on the standard temperature scaling rules of the building blocks (MM11, MM31).

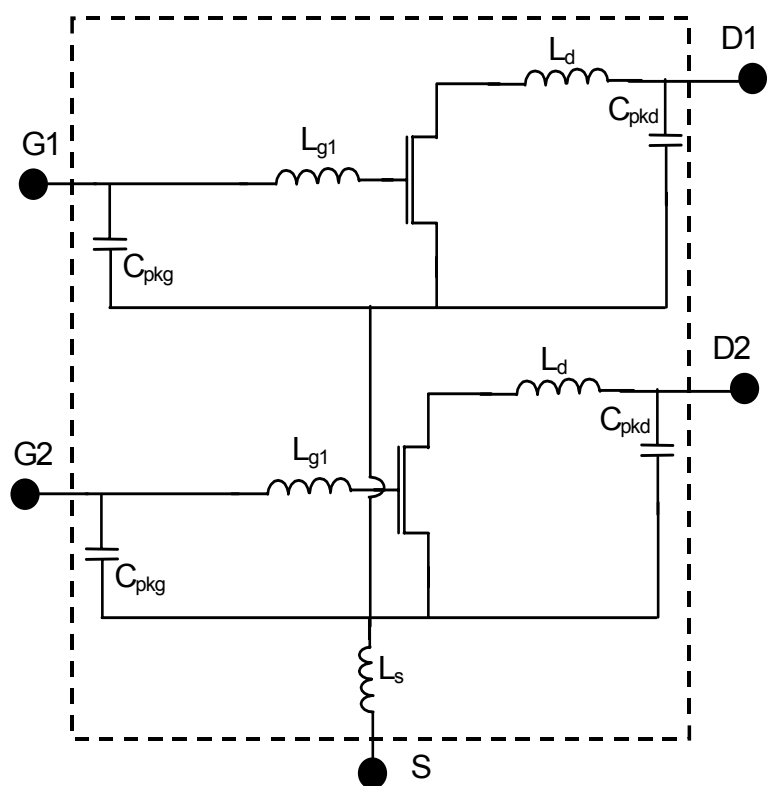
At present, lumped element components are used to model the matching capacitors, package parasitic capacitance and bond-wire inductances.

## 3. Model Parameters

The ADS symbol for the BLF574 device is shown in Fig 2.



**Fig 2.** ADS symbol of the BLF574 device model.



**Fig 3.** Schematic of the package model as in Fig 2.

The parameters  $L_{g1\_Spread}$ ,  $L_{g2\_Spread}$ , etc. allow controlling the spread of the values of the bond-wire inductances and matching capacitances. In practice, the parameters set the ratio between the actual and nominal values of each element<sup>2</sup>. By default, these parameters are set to 1.

2. For instance, by setting  $L_{g1\_spread}$  to 0.95, the actual value of the  $L_{g1}$  inductance becomes 95% its nominal value.

The expected statistical distributions of the spreading of the bond-wire inductances and matching capacitances are available and can be provided by NXP on special request.

The T\_Device parameter controls the device temperature used in the simulation.

## 4. Parameter extraction procedure

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The model parameters of each section were extracted with the following procedure:

- i. Extraction of the parameters of the active die model
  - a. The DC characteristics were measured in wide bias and temperature ranges ( $V_{gs}$  up to 15V,  $V_{ds}$  up to 30V, T up to 125 °C).
  - b. The s-parameter were measured in a wide frequency band
  - c. Dedicated structures were used for the de-embedding of the parasitics due to metal structures and interconnects from the s-parameter data.
  - d. A semi-automated procedure implemented with the Agilent's IC-CAP program was used to extract the model parameters
- ii. Extraction of the parameters of the package model
  - a. The values of the matching capacitances are obtained from design information
  - b. The value of the package parasitic capacitance is measured with a low-frequency CV meter
  - c. The starting values of the bond-wire inductances are obtained from design information.
  - d. The device S-parameters are measured using both an unmatched test fixture<sup>3</sup> and the application circuit.
  - e. The inductance values are then optimized by fitting the S-parameters data. The package parasitic source inductance is also optimized.

## 5. Model limitations

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The current version of the model includes only “static” thermal effects. This means that only the simulation temperature can be specified. As a consequence, it is expected that the model will provide a slight overestimation of the  $P_{1dB}$  and  $P_{3dB}$  values. The amount of this overestimation depends on the specific simulation conditions. However, it is expected not to exceed 1 dB.

Another consequence of the absence of electro-thermal effects is that the applied bias voltage ( $V_{gs}$ ) needed to obtain the required  $I_{dq}$  is expected to be 0.1V-0.2V higher in simulations than in measurements.

The absence of dynamic thermal effects also implies that the model is at present not capable to take in to account thermal memory effects.

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3. This test fixture is composed by a simple 50Ω transmission line and, therefore, provides 50Ω loadings at the input and output of the device.

In addition, since the model is based on a quasi-static formulation, it does not predict memory effects due to non-quasi-static (NQS) phenomena.

Some of these limitations will be overcome in the near future when a new, fully electro-thermal, version of the model (at present under testing) will be made available.

## 6. Installation Instructions

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In order to run properly, the Design Kit requires the latest version of the Philips model library SiMKit to be installed (see [Table 1](#) for version information). The SiMKit model library provides the definitions of the primitive submodels employed by the main device model. The installation procedure is described for three possible cases.

### 6.1 Case 1: No SiMKit installed

- i. Close all ADS schematics
- ii. In the main window of ADS, select "Design Kit -----> Install Design Kits....."
- iii. Install the Philips SiMKit
- iv. Exit and restart ADS
- v. In the main window of ADS, select "Design Kit -----> Install Design Kits....."
- vi. Install the model Design Kit
- vii. Exit and restart ADS
- viii. Now the model will function properly

### 6.2 Case 2: Old version of the SiMKit installed

- i. Close all schematics
- ii. In the main window of ADS, select "Design Kit -----> Setup Design Kits....."
- iii. REMOVE the older version of the SiMKit (DO NOT just DISABLE the old SiMKit)
- iv. Apply the changes
- v. Exit and restart ADS
- vi. In the main window of ADS, select "Design Kit -----> Install Design Kits....."
- vii. Install the Philips SiMKit
- viii. Exit and restart ADS
- ix. In the main window of ADS, select "Design Kit -----> Install Design Kits....."
- x. Install the model Design Kit
- xi. Exit and restart ADS
- xii. Now the model will function properly

### 6.3 Case 3: Updated version of the SiMKit installed

- i. Close all schematics
- ii. In the main window of ADS, select "Design Kit -----> Install Design Kits....."
- iii. Install the Design Kit of the model
- iv. Exit and restart ADS
- v. Now the model will function properly

**NOTE:** failing to have the proper version of the Philips SiMKit installed will result in an error message during the simulations.



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