

# R\_10032

CA-330-11; LDMOS bias module

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Report

## Document information

Info	Content
Keywords	LDMOS, bias
Abstract	This report describes a bias module for LDMOS RF power transistors. It provides a low-noise bias supply, temperature compensation, and a very low output impedance to help with video bandwidth optimisation



## Revision history

Rev	Date	Description
1.0	20120724	Initial version

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## 1. Introduction

LDMOS RF power transistors require temperature-compensated gate bias voltages to maintain constant quiescent drain currents over temperature. Additionally, the bias source must present a very low frequency to the LDMOS gate across the modulation frequency range ("video bandwidth") to minimize nonlinearity and memory effects.

This report describes a bias module for LDMOS RF power transistors. It provides a low-noise bias supply, temperature compensation, and a very low output impedance to help with video bandwidth optimization.

## 2. Summary

The characteristics of the bias module described in this report are summarized in [Table 1](#).

**Table 1. Summary of bias module characteristics**

Parameter	Value
Supply voltage	10 V to 80 V
Supply current	23 mA typical (no-load)
Output voltage	0 V to 3 V <sup>[1]</sup>
Output voltage adjustment range	1.4 V typical
Output voltage temperature compensation	−2 mV/°C typical <sup>[2]</sup>
Output voltage stability	≤ 500 μV
Output impedance	≤ 2.5 Ω, DC to 100 MHz
Output voltage noise	≤ 100 μV RMS, 10 Hz to 100 kHz
Output current	70 mA typical
Dimensions	26 mm × 11 mm × 8 mm

[1] Resistor values may have to be changed for part of range.

[2] Uses external NPN temperature sensing transistor in contact with heatsink.

## 3. Circuit description

### 3.1 Temperature compensation

The quiescent drain current  $I_{DQ}$  (and hence the operating point) of the RF device is set by adjusting the gate-source voltage  $V_{GS}$  with a constant-voltage bias source. In an LDMOS device, the gate-source threshold voltage  $V_{GS(th)}$  is inversely proportional to temperature, with a slope of about  $-2$  mV/°C. To maintain a constant quiescent current, the voltage generated by the bias supply should vary as a function of the junction temperature  $T_j$  of the RF device.

It is difficult to track the junction temperature exactly. However, reasonable results are obtained by monitoring the temperature of the baseplate, which is close to the RF transistor, with the temperature compensated bias circuit used in this amplifier. This circuit is shown in [Figure 1](#).

The temperature sensing device ( $Q_{temp}$ ), is attached to the baseplate near the RF device through a hole in the PCB. Its collector current is proportional to temperature, which results in a collector voltage slope of approximately  $-10\text{ mV}/^{\circ}\text{C}$ . Part of this temperature-dependent voltage is summed with the adjustable bias voltage from potentiometer R5 to generate the temperature-compensated final bias voltage.

### 3.2 Gate voltage adjustment

A variable voltage derived from the 8 V supply is summed with the temperature monitor voltage to generate a temperature-compensated gate voltage. R7 and R9 are selected to set the desired gate voltage trim range, and R10 is selected to provide the desired amount of temperature compensation. [Figure 1](#) shows component values for  $V_{GS} = 2.2 \pm 0.7\text{ V}$ , as given in [Figure 2](#).

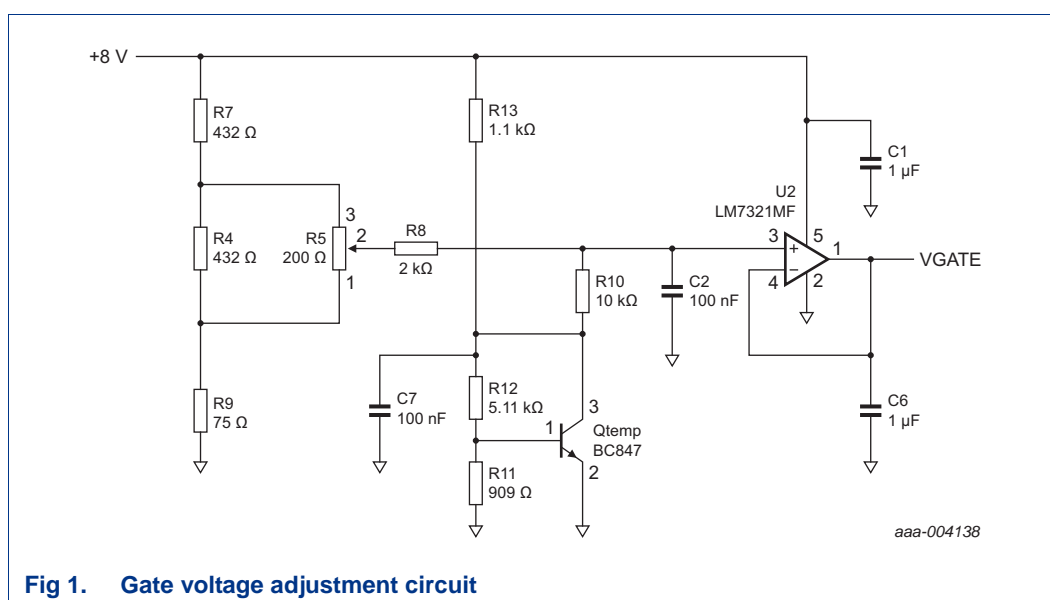
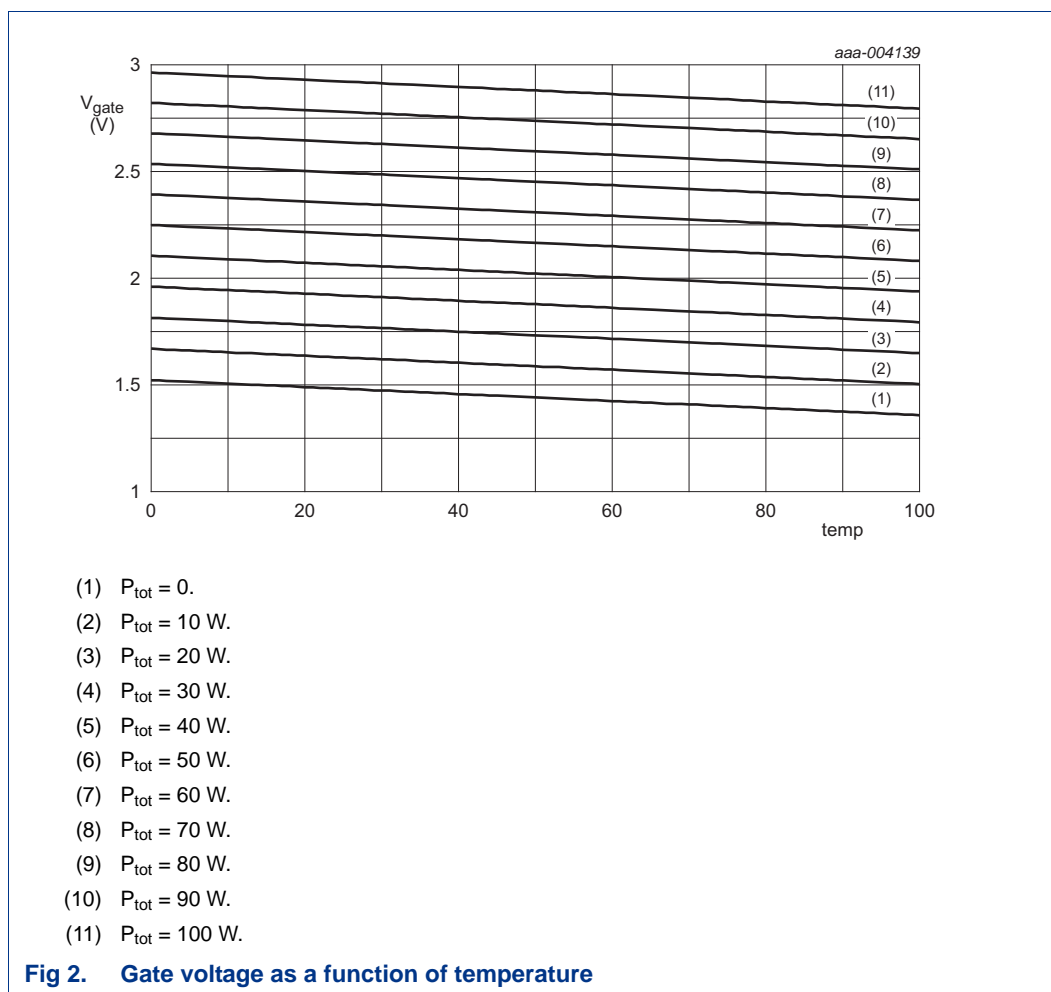


Fig 1. Gate voltage adjustment circuit



U2 is a high-current operational amplifier chosen because it is stable with any capacitive load. As shown in [Figure 3](#), the output impedance of the bias source is low (less than  $2.5 \Omega$ ) because of the feedback around U2. However, practical LDMOS applications may require an additional series gate resistor of  $5 \Omega$  to  $20 \Omega$  to ensure low-frequency device stability.

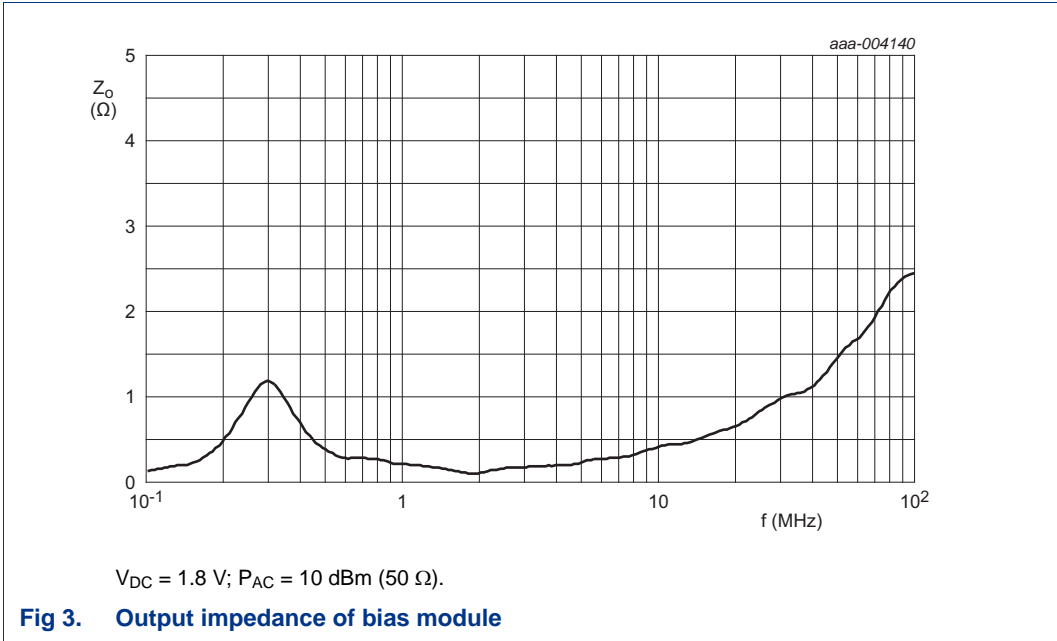


Fig 3. Output impedance of bias module

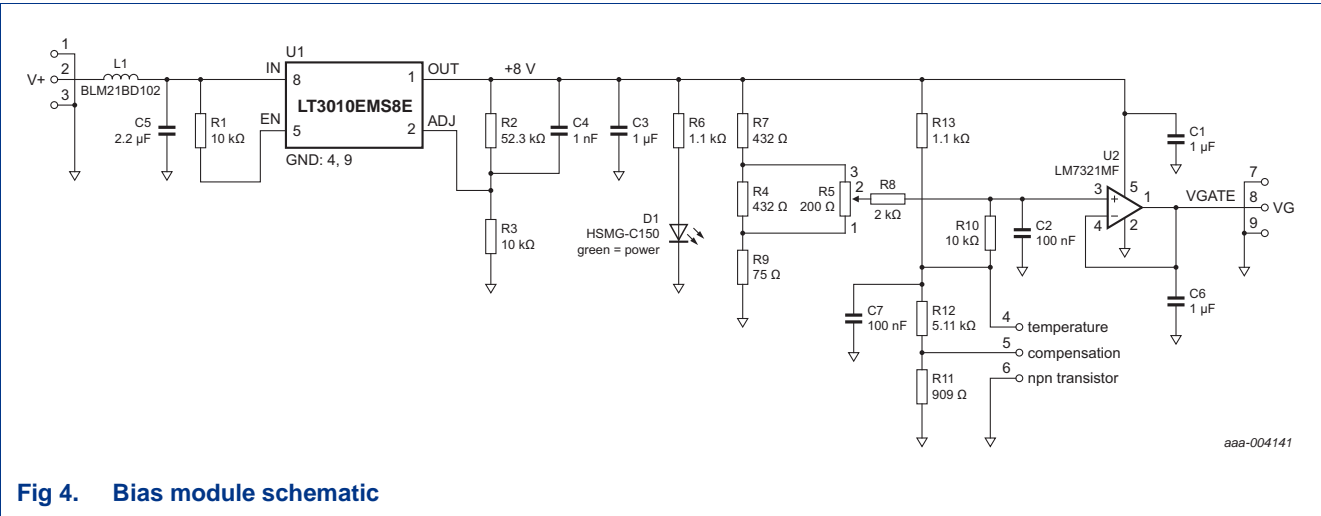


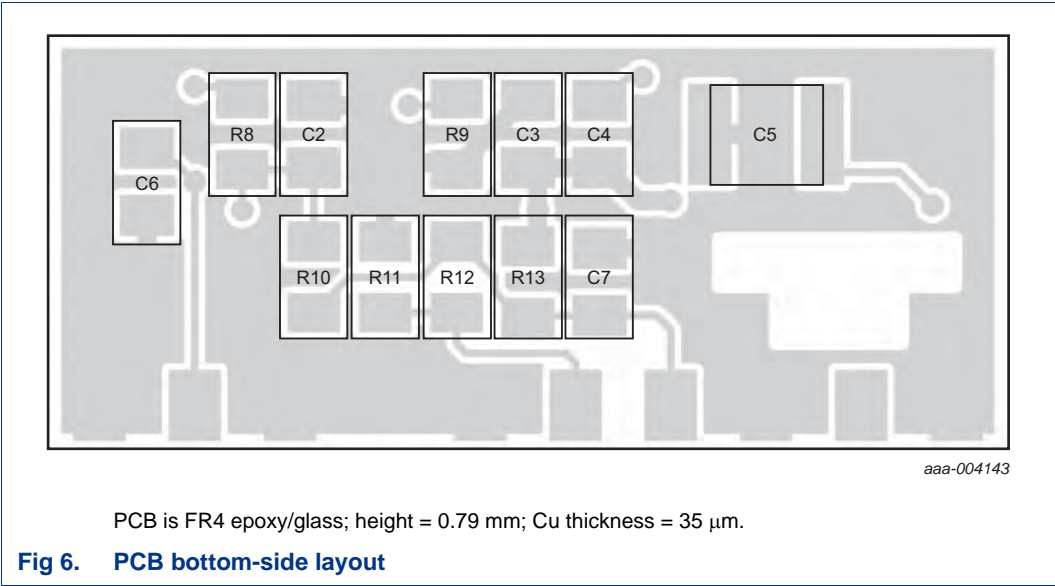
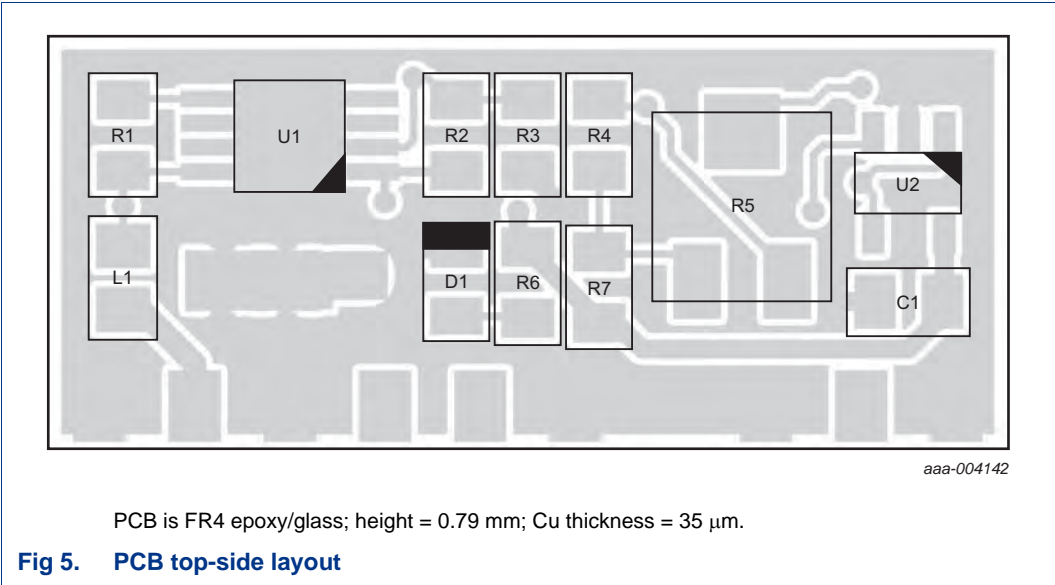
Fig 4. Bias module schematic

Table 2. Bias module bill of materials  
See [Figure 5](#) and [Figure 6](#) for component layout.

Component	Description	Value	Remarks
C1, C3, C6	capacitor; 50 V 10 % X7R, 0805	1 μF	
C2, C7	capacitor; 50 V 10 % X7R, 0805	100 nF	
C4	capacitor; 100 V 10 % NP0, 0805	1 nF	
C5	capacitor; 100 V 10 % X7R, 1210	2.2 μF	
D1	LED; green, 1206		
L1	ferrite bead; 200 mA, 0805		Murata BLM21BD102SN1D
R1, R3, R10	resistor; 1 % 100 ppm CF, 0805	10.0 kΩ	
R2	resistor; 1 % 100 ppm CF, 0805	52.3 kΩ	
R4, R7	resistor; 1 % 100 ppm CF, 0805	432 Ω	

Table 2. Bias module bill of materials ...continued  
See Figure 5 and Figure 6 for component layout.

Component	Description	Value	Remarks
R5	potentiometer; 5t cermet	200 $\Omega$	Bourns 3214J-1-201E
R6, R13	resistor; 1 % 100 ppm CF, 0805	1.10 k $\Omega$	
R8	resistor; 1 % 100 ppm CF, 0805	2.00 k $\Omega$	
R9	resistor; 1 % 100 ppm CF, 0805	75 $\Omega$	
R11	resistor; 1 % 100 ppm CF, 0805	909 $\Omega$	
R12	resistor; 1 % 100 ppm CF, 0805	5.11 k $\Omega$	
U1	voltage regulator, 3 V to 80 V adjustable, 50 mA, MSOP8		Linear LT3010EMS8E
U2	Op amp, rail-rail unlimited C <sub>load</sub> , SOT23-5		National LM7321MF



## 4. Abbreviations

Table 3. Abbreviations

Acronym	Description
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
PCB	Printed-Circuit Board



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