



Logic Demo Board Kit

Compact, easy-to-use boards for fast, simple test and evaluation

www.nxp.com

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Innovation starts here



Benefits of using NXP logic

- ▶ Longer battery life
- ▶ Lower chip count
- ▶ Low overall system power consumption
- ▶ Easy placement in tighter layouts
- ▶ Environmentally friendly products

This kit includes compact, easy-to-use demo boards that make it simple to test and demonstrate some of our most innovative logic products. The table of contents appears on the following page.

Commitment and dedication

NXP is deeply committed to the logic market and continually invests in new process and package technologies, along with new packaging technologies, to ensure that our portfolio remains leading-edge. We offer a very broad variety of innovative products, ranging from state-of-the-art solutions for emerging applications to specialty functions and proven, mature solutions that enhance virtually any application.

Family	Features
LVC (Low Voltage CMOS)	Adds to the LV family with the following: <ul style="list-style-type: none">▶ Oversupply voltage tolerance up to 5.5 V▶ High speed (2 ns typ)
AUP (Advanced Ultra-low Power)	<ul style="list-style-type: none">▶ Lowest static and dynamic power consumption▶ Extremely small MicroPak and PicoGate packages▶ Single-, dual-, and triple-gate functions▶ Schmitt-trigger action▶ Very low leakage current in OFF mode▶ Extended temp range (-40 to 125 °C)

Wideband analog switches

The LVC SPST switches included in this demo kit deliver reduced signal loss, high bandwidth, and minimal distortion. They are ideally suited for use with analog and digital signals.

Product	-3 dB bandwidth	R_{ON} (typ) @ $V_{CC} = 3\text{ V}$
LVCV2G66	200 MHz @ 600 Ω	8.3 Ω
LVC2G66	400 MHz @ 50 Ω	7.8 Ω

Low-ohmic analog switch optimized for audio

The NX3L2G66, with its minimal voltage drop across the switch, delivers optimized performance in audio applications.

Product	-3 dB bandwidth	R_{ON} (typ) @ $V_{CC} = 3\text{ V}$
NX3L2G66	60 MHz @ 50 Ω	0.5 Ω

Demo boards included in this kit

Wideband analog switches

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Low-ohmic analog switch

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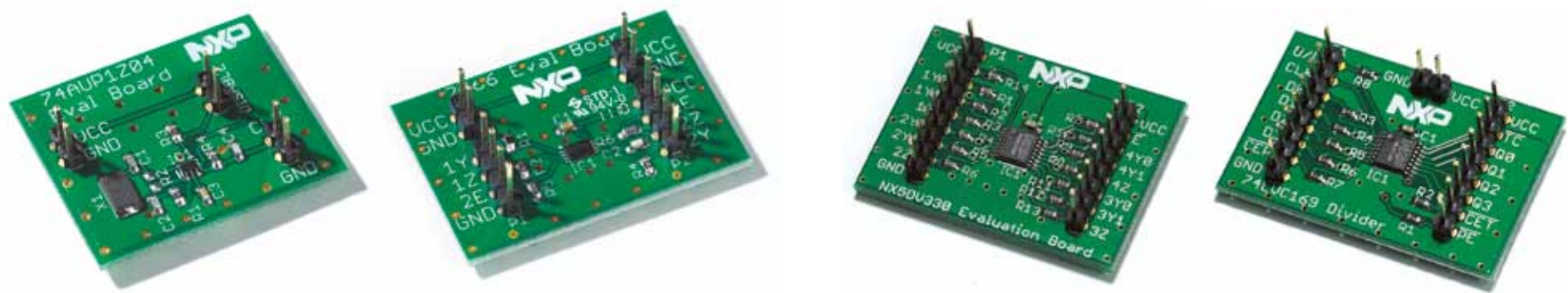
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NXP 74LVC2G66 demo board

This compact board makes it easy to demonstrate the 74LVC2G66, a dual SPST analog switch that supports high-frequency bandwidth and has control inputs tolerant to oversupply voltage.

Key features and benefits

- ▶ Wide supply voltage range (1.65 to 5.5 V) and low R_{ON} (5 Ω typ) for design flexibility
- ▶ High bandwidth (up to 500 MHz) for data-rich applications
- ▶ High speed with low propagation delay (0.4 ns typ)
- ▶ Ability to monitor I/O rise/fall times, plus propagation delays with different loads (capacitors and resistors)
- ▶ Oversupply voltage tolerance up to 5.5 V for enable inputs
- ▶ Low ON state capacitance (9.5 pF typ) for better signal integrity
- ▶ Fully specified for use in harsh conditions (-40 to +85 or +125 °C)
- ▶ Excellent ESD performance (7.5 kV HBM), suitable for consumer applications
- ▶ Switch current capability of 32 mA
- ▶ Available in very small leadless packages for PCB savings

Applications

- ▶ Portable devices
- ▶ Industrial
- ▶ Automotive
- ▶ Computing
- ▶ Consumer

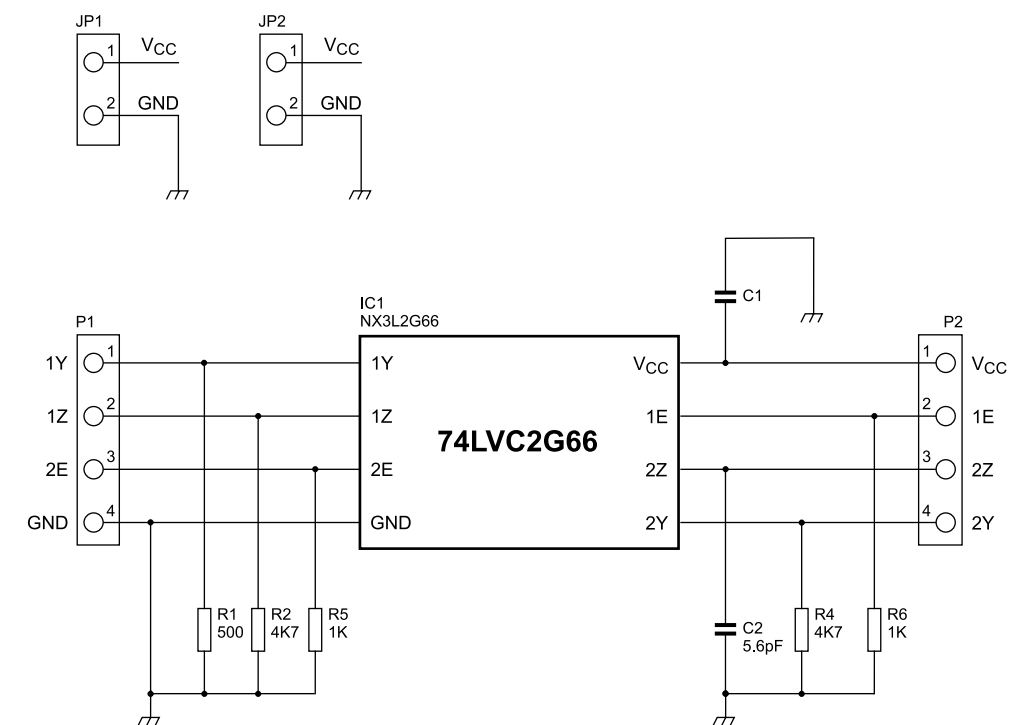
The 74LVC2G66 provides two single-pole, single-throw (SPST) analog switch functions. Each switch has two I/O terminals (nY and nZ) and one active HIGH enable input (nE). When nE is LOW, the analog switch is turned off. Schmitt-trigger action at the enable inputs makes the circuit tolerant of slower input rise and fall times across the entire V_{CC} range, from 1.65 to 5.5 V.

Schematics of the 74LVC2G66 demo board are shown in the figure below. A supply voltage of 1.65 to 5.5 V can be used for the board. Signals in the range of 0 V to V_{CC} can be connected to the nY pins and switched to output to the nZ pins (and vice versa) with minimal loss. There are two channels in the 74LVC2G66 switch. The maximum input frequency for each channel can be as high as 500 MHz at a load of 50 Ω and 5 pF. A decoupling capacitor of 0.1 μ F is connected between the V_{CC} and GND pins to smooth out the power rail. By default, 1 k Ω pull-down resistors are connected between the 1E, 2E lines and GND to avoid floating Enable pins. Both switches are OFF/ open.

Demonstrate fast switching of HF signals with a dual SPST analog switch

To turn a switch ON (close the contact), a logic HIGH signal needs to be connected to the respective Enable pin. To connect the Enable pins and GND leads of an oscilloscope probe to the board, additional connectors

(JP1 and JP2) with V_{CC} and GND pins are provided. Also, loads of $R1 = 500 \Omega$, $R2 = R4 = 4.7 \text{ k}\Omega$ and $C2 = 5.6 \text{ pF}$ are provided so designers can see variations in the output rise and fall times at resistive and capacitive loads.



Circuit schematic of 74LVC2G66 demo board

Test results

Results of testing done on the 74LVC2G66 demo board are shown in the figures below. In Figure 1, the purple waveform is a 500 kHz square wave input with an amplitude of 3 V applied at the 1Z pin, and the green waveform is the switch output at the 1Y pin with a load of 500 Ω when the Enable pin (1E) is pulled high to 3 V and the switch is ON. The supply voltage V_{CC} for the switch is 3 V. In Figure 2, the green waveform shows the output at the 1Y pin when Enable pin (1E) is connected to GND and the switch is OFF. The supply voltage V_{CC} for the switch is

still 3 V, and the purple input signal at the 1Z pin is 3 V. In Figure 3, the purple waveform shows a 5 MHz input signal of 3 V at the 1Z input, and the green waveform is the output of approx. 2.84 V at the 1Y output when the supply voltage V_{CC} is 3 V and the 1E pin is at a logic HIGH level of 3 V. In Figure 4, the purple waveform is a 3 V input signal with a 5 MHz frequency at the 1Z input of the switch, and the green waveform is an approx. 97 mV signal at the 1Y output when the V_{CC} is 3 V and the 1E pin is pulled LOW to GND.

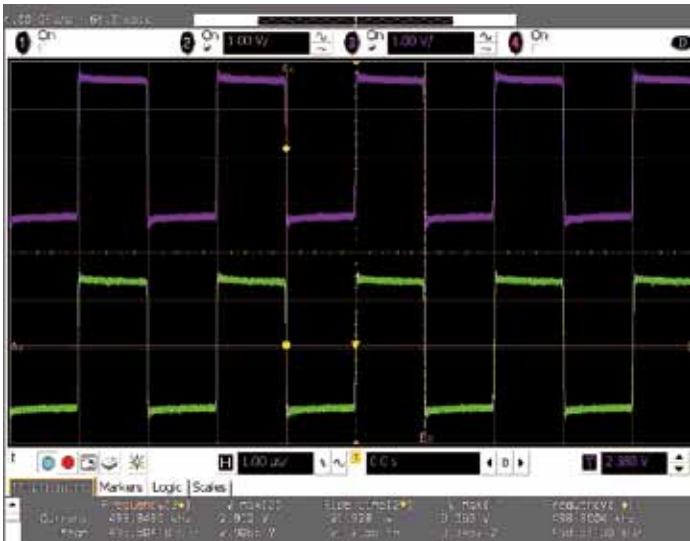


Figure 1

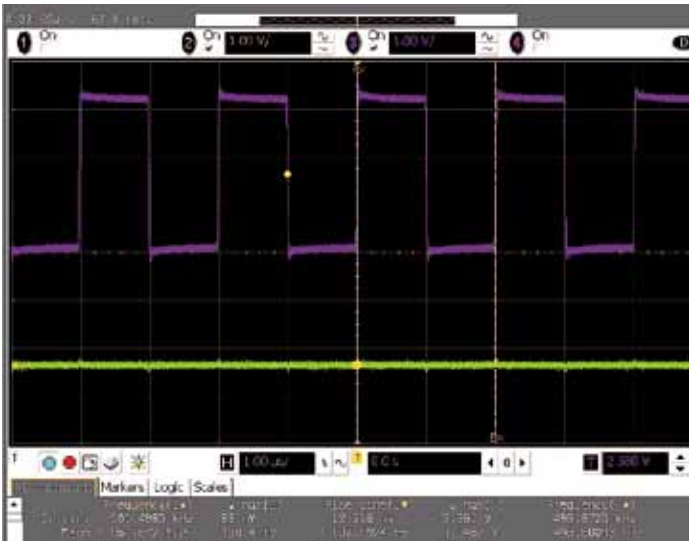


Figure 2







Figure 3



Figure 4

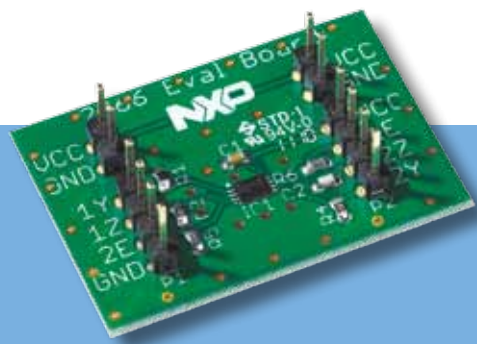
Packages

The 74LVC2G66 is available in leadless 8-pin XSON, XSONU, and XQFN packages and in standard 8-pin TSSOP and VSSOP packages.

Package suffix	DP	GD	GT	GM	DC
					
	SOT505-2	SOT996-2	SOT833-1	SOT902-1	SOT765-1
	8-pin	8-pin	8-pin	8-pin	8-pin
Width (mm)	3	2	2	1.65	2
Length (mm)	3	3	1.05	1.65	2.3
Height (mm)	1.1	0.5	0.5	0.5	1
Pitch (mm)	0.65	0.5	0.5	0.5	0.5

Ordering information

Part number	Package				
	Temp. range	Name	Type	Marking	Material
74LVC2G66DP	-40 to 125 °C	TSSOP8	Thin shrink small outline package	V66	Plastic
74LVC2G66GD	-40 to 125 °C	XSON8U	Extremely thin small outline package; no leads	V66	Plastic
74LVC2G66DC	-40 to 125 °C	VSSOP8	Very thin shrink small outline package	V66	Plastic
74LVC2G66GT	-40 to 125 °C	XSON8	Extremely thin small outline package; no leads	V66	Plastic
74LVC2G66GM	-40 to 125 °C	XQFN8U	Extremely thin quad flat package; no leads	V66	Plastic



NXP 74LVCV2G66 demo board

Use this compact board to demonstrate the 74LVCV2G66, a dual single-pole single-throw switch (SPST) analog switch with high-frequency bandwidth and over supply voltage tolerant control and data inputs.

Key features and benefits

- ▶ Wide supply voltage range (2.3 to 5.5 V)
- ▶ Low R_{ON} (7.5 Ω typ) for design flexibility
- ▶ High bandwidth (up to 210 MHz) for data-rich applications
- ▶ Oversupply voltage tolerance up to 5.5 V for switch and enable inputs
- ▶ Ability to monitor speed with lower propagation delay (0.4 ns typ)
- ▶ Ability to monitor I/O rise/fall times and propagation delay with different loads (capacitors and resistors)
- ▶ Low ON state capacitance (16 pF typ) for greater signal integrity
- ▶ Very small leadless packages for reduced PCB space
- ▶ Fully specified for use in harsh conditions (-40 to +85 or +125 °C)

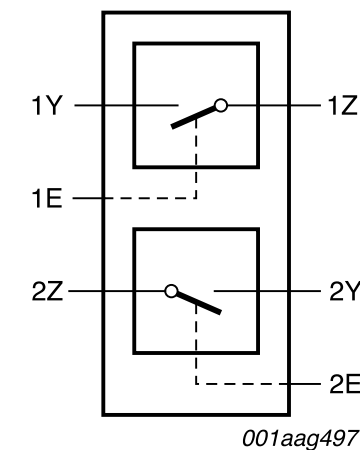
Applications

- ▶ Portable devices
- ▶ Industrial
- ▶ Automotive

The 74LVCV2G66 provides two low-ohmic SPST analog switch functions. Each switch includes an overvoltage-tolerant input/output terminal (pin nZ), an output/input terminal (pin nY) and a low-power active HIGH enable input (pin nE). The overvoltage-tolerant switch terminals allow the switching of signals in excess of V_{CC} . The low-power enable input eliminates the need to use current-limiting resistors in portable applications when using control logic signals much lower than V_{CC} . These inputs are also overvoltage-tolerant.

A supply voltage of 2.3 to 5.5 V can be used for board. Signals in the range of 0 V to V_{CC} can be connected to nY pins and switched to output nZ pins with minimal loss. However, signals in excess of V_{CC} up to 5.5 V can be applied to nZ pins and switched to nY pins with minimal loss.

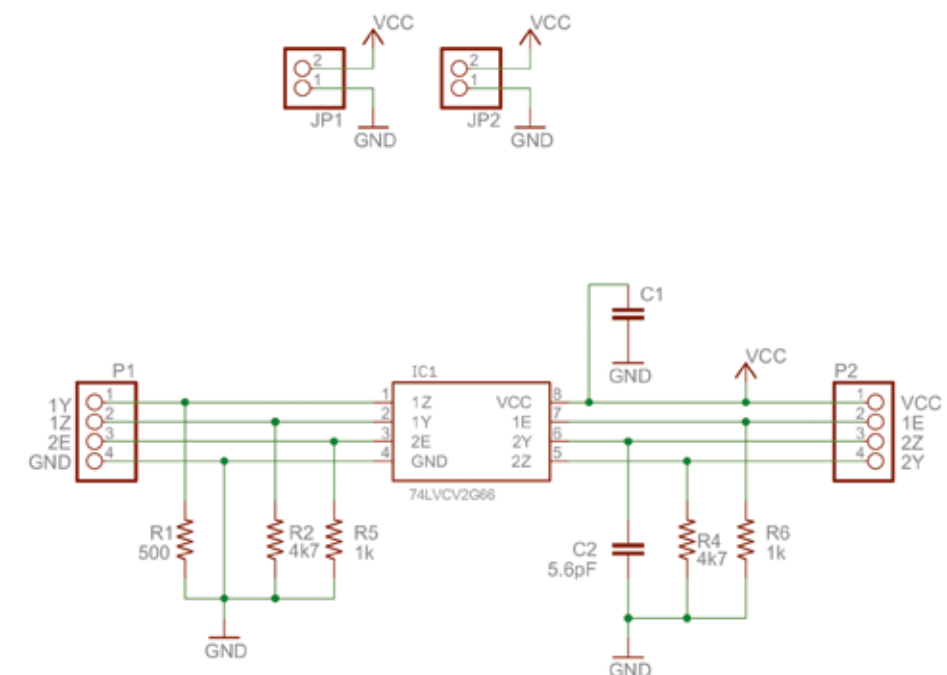
Demonstrate fast switching of oversupply voltage signals with dual SPST analog switch



74LVCV2G66 functional block diagram

There are two channels in the 74LVCV2G66 switch. The maximum input frequency for each channel can be as high as 210 MHz at a load of 600 Ω and 50 pF. By default, 1 k Ω pull-down resistors are connected from the 1E and 2E lines to GND to avoid floating enable pins, and both switches are OFF/open. In order to turn a switch ON (close the contact), a logic high signal needs to be connected to the respective enable pin. Additional connectors (JP1 and JP2) with V_{CC} and GND pins are provided to support easy connection of the enable pins and GND leads of oscilloscope probes to the board. Also, loads of $R1 = 500 \Omega$, $R2 = R4 = 4.7k\Omega$, and $C2 = 5.6 \text{ pF}$ are provided so designers can view variations in output rise and fall times at resistive and capacitive loads.

To save PCB space, the 74LVCV2G66 switch is available in leadless 8-pin XSON and XQFN packages.



Circuit schematics 74LVCV2G66 demonstration board

Test results

The figures below present the results of tests done on the 74LVCV2G66 demo board. The purple waveform in Figure 1 is a 12.5 kHz square wave input with amplitude of 5.21 V applied at the 1Z pin, while the green waveform is the switch output at 1Y pin with a load of 4.7 kΩ when the enable pin (1E) is pulled high to 3 V and the switch is ON. The switch’s supply voltage V_{CC} is 3 V. Figure 2 shows the output at 1Y pin in the green waveform, when the enable pin (1E) is connected to GND and the switch is OFF. The switch’s supply voltage V_{CC} remains at 3 V. The purple input signal at 1Z pin is 5.38 V.

In Figure 3, the purple waveform shows a 50 kHz input signal of 5.16 V at the 2Z input, while the green waveform indicates

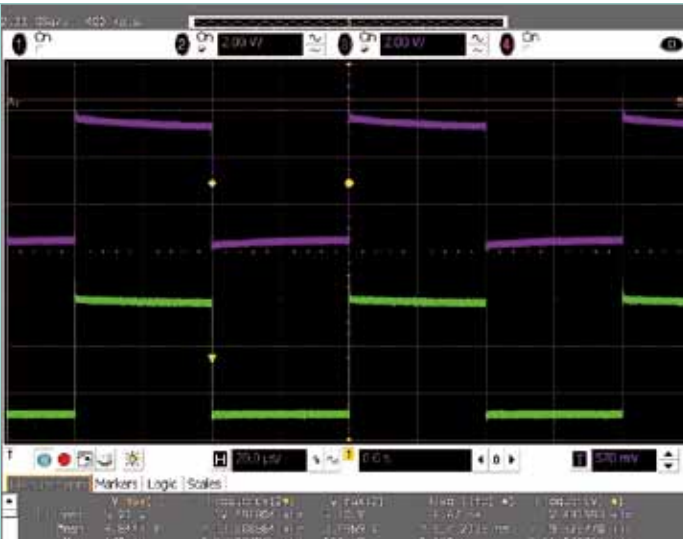


Figure 1

the output of approximately 4.97 V at the 2Y output when the supply voltage V_{CC} is 3 V and the 2E pin is at a logic HIGH level of 3 V.

The purple waveform in Figure 4 shows a 2.64 V input signal with 5 MHz frequency at the 1Z input. The green waveform is a 2.57 V signal at the 1Y output, when V_{CC} is 3 V and the 1E pin is pulled HIGH to V_{CC} . The load used for the 1Y output is 4.7 kΩ.

Note that in all test conditions there is minimal loss in signal amplitude between the input and output terminals of each switch.

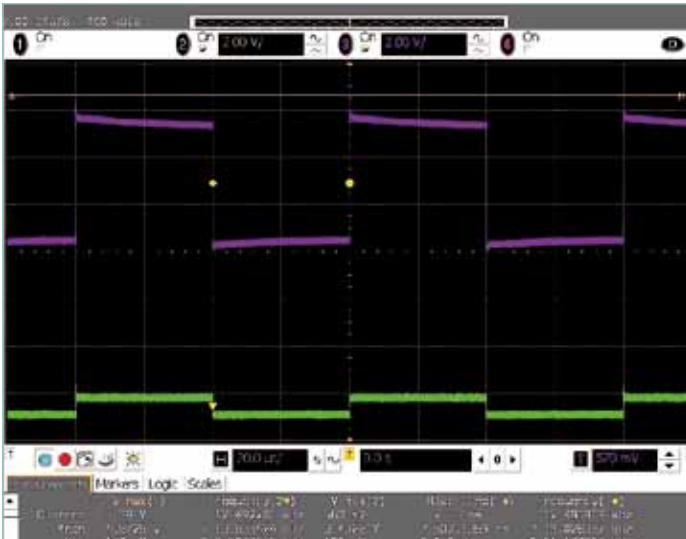


Figure 2

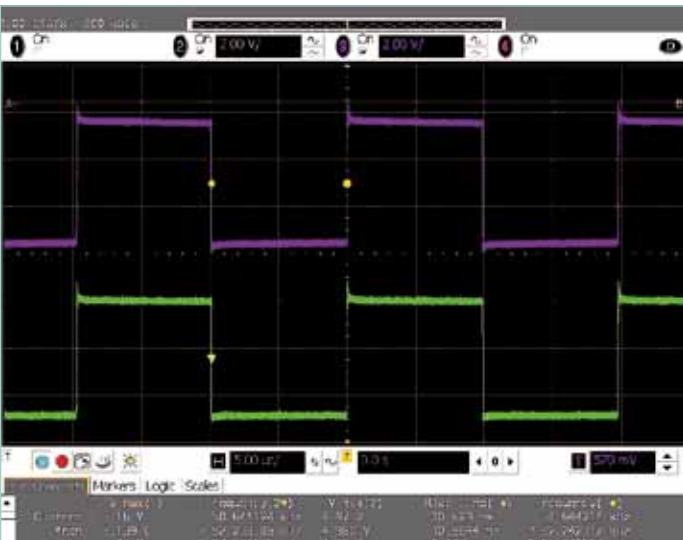





Figure 3



Figure 4

Packages

The 74LVCV2G66 is available in 8-pin TSOP, VSSOP, and leadless XSON packages.

Package suffix	DP	GD	DC
			
	SOT505-2	SOT996-2	SOT765-1
	8-pin	8-pin	8-pin
Width (mm)	3	2	2
Length (mm)	3	3	2.3
Height (mm)	1.1	0.5	1
Pitch (mm)	0.65	0.5	0.5

Ordering information

Part number	Package				
	Temp. range	Name	Type	Marking	Material
74LVCV2G66DP	-40 to 125 °C	TSSOP8	Thin shrink small outline package	Y66	Plastic
74LVCV2G66GD	-40 to 125 °C	XSON8U	Extremely thin small outline package; no leads	Y66	Plastic
74LVCV2G66DC	-40 to 125 °C	VSSOP8	Very thin shrink small outline package	Y66	Plastic



NXP NX3L2G66 demo board

Demonstrate lossless signal switching with a dual low-ohmic SPST analog switch

Use this compact board to demonstrate the NX3L2G66, a low-ohmic, dual single-pole single-throw (SPST) analog switch.

Key features and benefits

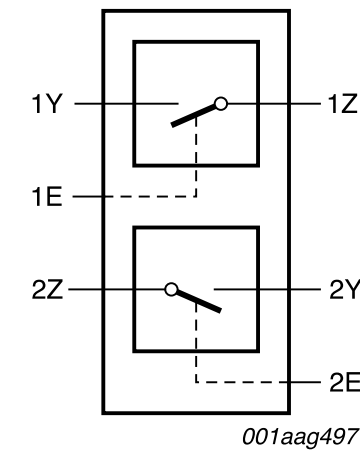
- ▶ Wide supply voltage range (1.4 to 4.3 V) and low R_{ON} (0.5 Ω typ) for design flexibility
- ▶ High current handling capability (up to 350 mA continuous) for different load types
- ▶ Ideal for sensing and sampling applications with low leakage (<50 nA at +85 °C)
- ▶ Overvoltage-tolerant control inputs, eliminating the need for an external voltage translator
- ▶ High off isolation (90 dB) for better protection of devices in circuit
- ▶ Ability to monitor the I/O rise/fall times and propagation delays with different loads (capacitors and resistors)
- ▶ Excellent ESD performance (7.5 kV HBM), suitable for consumer applications
- ▶ Available in very small 8-pin leadless XSON and XQFN packages for reduced PCB size
- ▶ Fully specified for use in harsh conditions (-40 to +85 or +125 °C)

Applications

- ▶ Portable devices
- ▶ Industrial
- ▶ Automotive

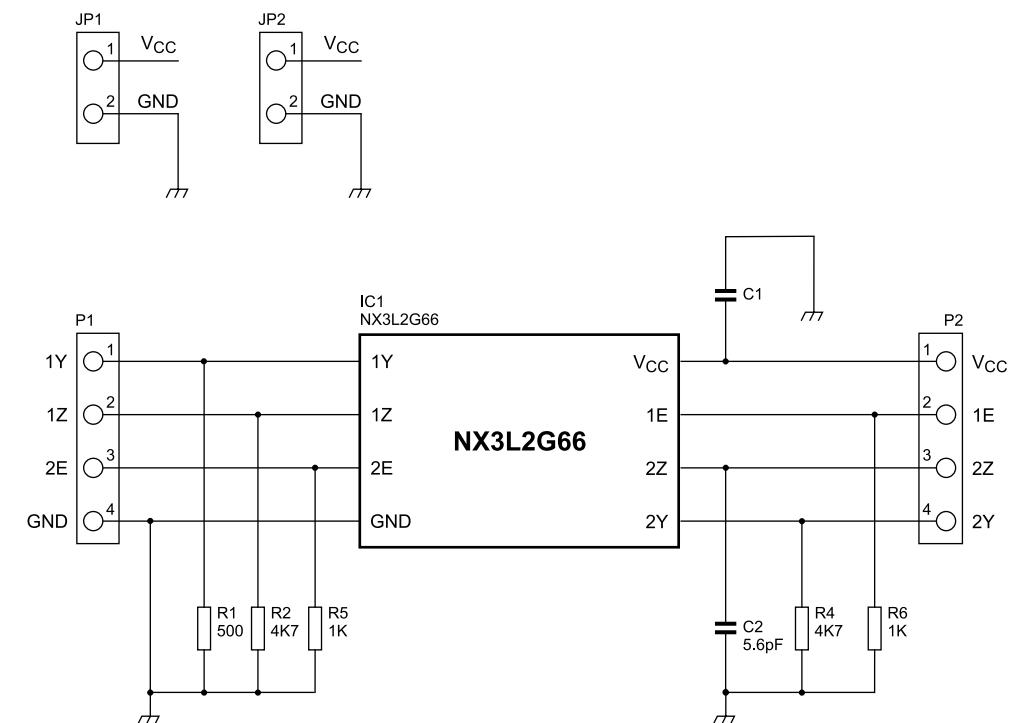
Each switch in the NXP NX3L2G66 has two I/O terminals (nY and nZ) and an active HIGH enable input (nE). When pin nE is LOW, the analog switch is turned off.

Schmitt-trigger action at the enable input (nE) makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range (1.4 to 4.3 V). The NX3L2G66 allows signals with amplitude up to V_{CC} to be transmitted from nY to nZ or from nZ to nY. The low ON resistance (0.5 Ω) and flatness (0.13 Ω) ensure minimal attenuation and distortion of transmitted signals.



NX3L2G66 functional block diagram

A supply voltage of 1.4 to 4.3 V can be used for the board. Signals in the range of 0 V to V_{CC} can be connected to nZ pins and switched to nY pins or vice versa with minimal loss. The maximum input frequency for each of the two channels can be as high as 60 MHz at a load of 50 Ω . By default, to avoid floating enable pins, 1 k Ω pull-down resistors are connected between the 1E, 2E lines and GND, and both switches are OFF/ open. In order to turn a switch ON (close the contact), a logic HIGH signal needs to be connected to the associated Enable pin. Additional connectors (JP1 and JP2) with V_{CC} and GND pins make it easy to connect the Enable pins and GND leads of an oscilloscope probe to the board. Also, to test variations in output rise and fall times at resistive and capacitive types of loads, the board supports loads of $R1 = 500 \Omega$, $R2 = R4 = 4.7 \text{ k}\Omega$, and $C2 = 5.6 \text{ pF}$.



Circuit schematic of NX3L2G66 demo board

Test results

The figures below present the results of tests done on the NX3L2G66 demo board. The purple waveform in Figure 1 is a 500 kHz square wave input with amplitude of 1.71 V applied at the 1Z pin, while the orange waveform is the switch output at 1Y pin with a load of 500 Ω, when Enable pin (1E) is pulled LOW and switch is OFF. Figure 2 shows the output at 1Y pin in the orange waveform, when Enable pin (1E) is connected to a switch supply voltage V_{CC} of 3 V.



Figure 1

Figures 3 and 4 show the same test results for pins 2Y (used as input) and 2Z (used as output) but the output load is changed to 5.6 pF. Again, the purple waveforms in Figures 3 and 4 show the input signals and the orange waveforms show the switch output signals. Note that there is minimal loss in signal amplitude at the input and output terminals of each switch. Also, there is minimal change in the output rise and fall times and the frequency of the input and output signals at resistive and capacitive loads.

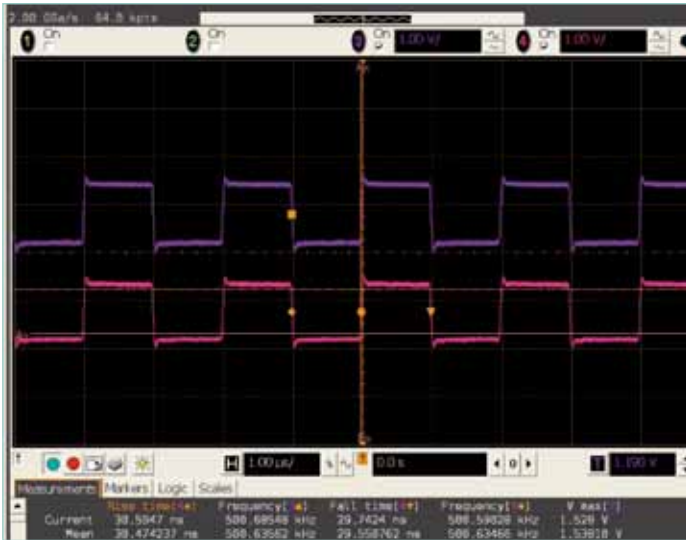


Figure 2

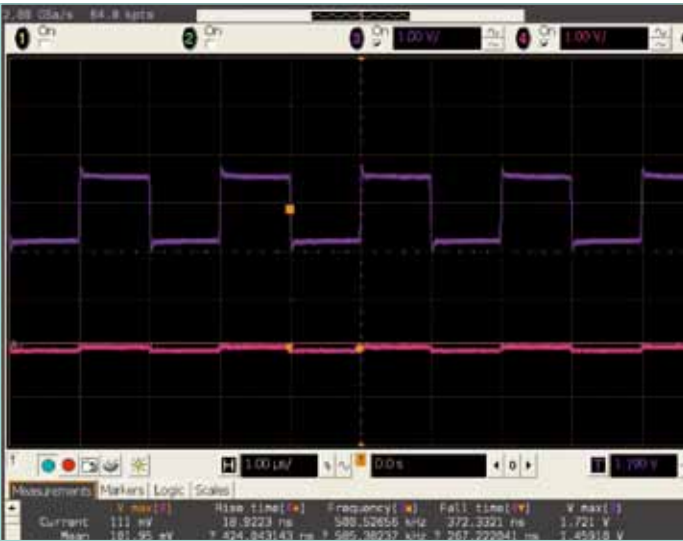


Figure 3



Figure 4

Packages

The NX3L2G66 is available in leadless 8-pin XSON, XSONU, and XQFN packages.

Package suffix	GT	GD	GM
			
	SOT833-1	SOT996-2	SOT902-1
	8-pin	8-pin	8-pin
Width (mm)	1.0	2	1.65
Length (mm)	1.95	3	1.65
Height (mm)	0.5	0.5	0.5
Pitch (mm)	0.5	0.5	0.5

Ordering information

Part number	Package				
	Temp. range	Name	Type	Marking	Material
NX3L2G66GT	-40 to 125°C	XSON8	Extremely thin small outline package; no leads	D66	Plastic
NX3L2G66GD	-40 to 125°C	XSON8U	Extremely thin small outline package; no leads	D66	Plastic
NX3L2G66GM	-40 to 125°C	XQFN8U	Extremely thin quad flat package; no leads	D66	Plastic



NXP NX5DV330 demo board

Demonstrate high-fidelity video with a wideband mux/demux

Use this compact board to demonstrate the NX5DV330, a quad 1-of-2 high-speed TTL-compatible video multiplexer/demultiplexer with low ON resistance.

Key features and benefits

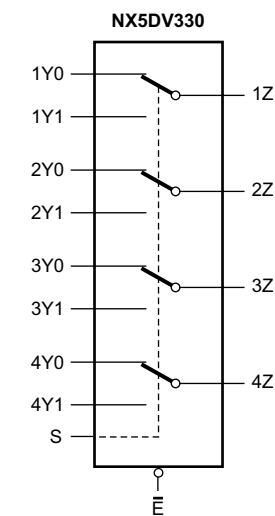
- Higher signal bandwidth for more details and higher fidelity in images
- Schmitt trigger at control inputs to better tolerate slow edges
- Low R_{ON} (5 Ω typ) for high-quality colors with higher dynamic range
- Low R_{ON} for low voltage drop across the switch and reduced signal attenuation
- Low R_{ON} flatness for reduced total harmonic distortion
- Low leakage current and high isolation for noise-free images
- Low cross-talk for low interference between active and idle display terminals
- Bidirectional design results in easy PCB layout for mux/demux applications
- Low supply current for reduced power consumption
- Low differential phase offset for low output skew
- TTL-compatible inputs for mixed CMOS/TTL designs
- High isolation between I/O pins to prevent false switching
- Available in very small 16-pin leadless DQFN package

Applications

- Portable devices
- Industrial
- Automotive

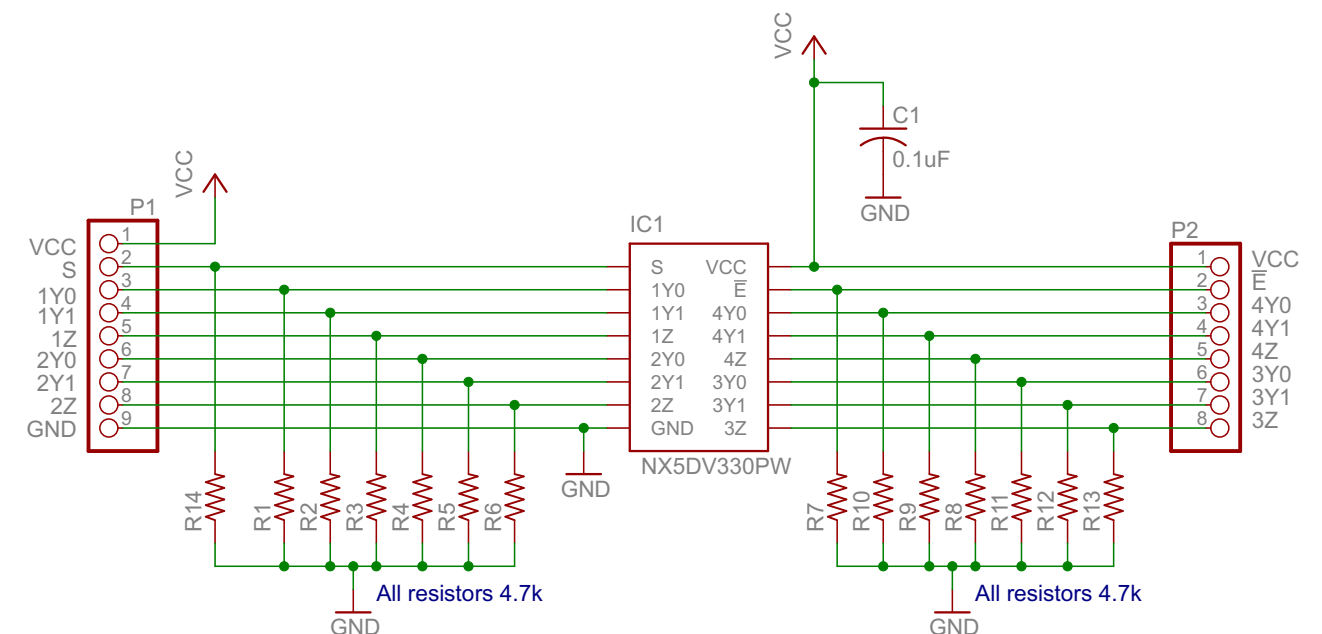
The NX5DV330 is ideal for switching analog and digital video signals and offers -3 dB bandwidth of 300 MHz at a load of 150 Ω . Analog VGA signals can be switched from a video source to either of two external monitors with minimal loss, up to a screen resolution of 1900 x 1200 pixels at a 75 Hz refresh rate. The low ON resistance allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. It has a digital select input (S), four independent inputs/outputs (nY0, nY1), a common input/output (nZ) and an active LOW enable input (\bar{E}). When pin \bar{E} is HIGH, the switch is turned off.

Schmitt-trigger action at the enable input (\bar{E}) and select input (S) makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range of 4.0 to 5.5 V. The NX5DV330 is characterized for operation from -40 to +85 $^{\circ}\text{C}$.



NX5DV330 functional block diagram

Schematics of the NX5DV330 demo board are shown below. A supply voltage of 4 to 5.5 V can be used for the board. Video and data signals with amplitude in the range of 0 V to V_{CC} can be connected to pins nZ and switched between pins nY0 and nY1 with minimal loss, based on the logic level of select pin S. Similarly, the voltage signals from two sources can be connected to pins nY0 and nY1 and pins nZ will multiplex the signals based on the logic level of select pin S. There are four channels in the NX5DV330 switch. The maximum input frequency for each channel can be as high as 300 MHz. By default, the Enable pin (active low) is pulled LOW to enable the switch. All four of the switch's channels can be turned off (inputs and outputs in high impedance), if a logic high signal is connected to the Enable pin.



Circuit schematic of NX5DV330 demo board

Test results

The figures below present the results of tests done on the NX5DV330 demo board. In Figure 1, the purple waveform is a 500 kHz square wave input with amplitude of 3.86 V applied at pin1Z and the green waveform is a 3.76 V switch output at 1Y0 pin, keeping the select pin S at GND.

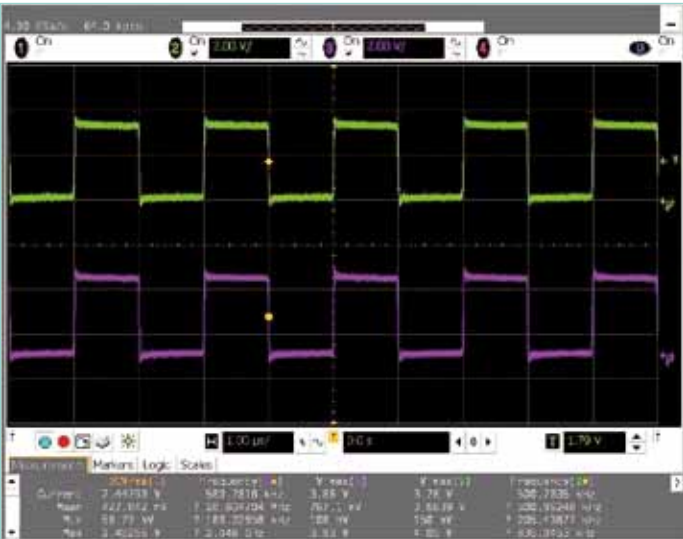


Figure 1

Figure 2 shows the output at pin 1Y0 in purple waveform and input at pin 1Z in green, when the select pin S is connected to V_{CC}. Figures 3 and 4 show the same test results for pins 4Z and 4Y0 but the frequency of input signal is increased to 5 MHz. The purple waveforms show the input signals and the green waveforms show the switch output signals.



Figure 2

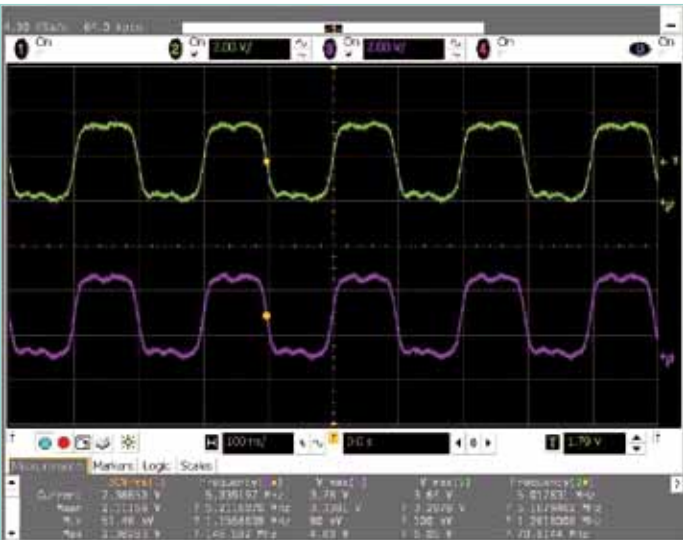


Figure 3

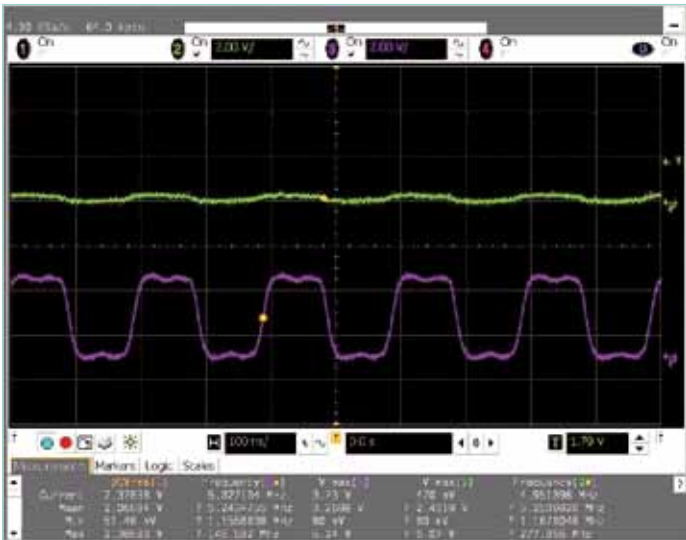


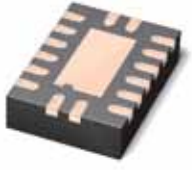



Figure 4

Packages

The NX5DV330 is available in 16-pin SO, SSOP/QSOP, TSSOP, and leadless DQFN packages.

Package suffix	D	PW	BQ	DS
				
	SOT109-1	SOT403-1	SOT763-1	SOT519-1
	16-pin	16-pin	16-pin	16-pin
Width (mm)	6.0	6.4	2.5	6
Length (mm)	9.9	5.0	3.5	4.9
Pitch (mm)	1.27	0.65	0.5	0.635

Ordering information

Part number	Package				
	Temp. range	Name	Type	Marking	Material
NX5DV330D	-40 to 85 °C	SO16	Small outline	NX5DV330D	Plastic
NX5DV330DS	-40 to 85 °C	SSOP16	Shrink small outline	X5DV330	Plastic
NX5DV330PW	-40 to 85 °C	TSSOP16	Thin shrink small outline	X5DV330	Plastic
NX5DV330BQ	-40 to 85 °C	DHVQFN16	Dual in-line compatible thermal enhanced very thin quad flat package with no leads	5DV330	Plastic



NXP AUP1Z04 demo board

Use this compact board to demonstrate the 74AUP1Z04, a low-power X-tal driver with enable and internal transistor.

Key features and benefits

- Wide supply voltage range: 0.8 to 3.6 V
- High noise immunity
- Inputs accept voltages to 3.6 V
- No need for external biasing resistor
- Partial power-down mode
- Low noise overshoot and undershoot: <10 % of V_{CC}
- Specified from -40 to +85 or +125 °C
- Reduced power consumption
- Fewer external components
- Stable operation over a wide range of conditions
- Increased flexibility in design and test
- Very small footprint and availability in leadless MicroPak packages

Applications

- Portable devices
- Industrial
- Automotive

The 74AUP1Z04 is a low-power X-tal driver optimized for use in crystal oscillator applications. It combines the functions of the 74AUP1GU04 and the 74AUP1G04, thus delivering the benefits of a compact footprint, lower power dissipation, and stable operation over a wide range of frequency and temperature. The 74AUP1Z04 also integrates output enable circuitry and an internal bias resistor. The output enable circuitry saves power, while the internal bias resistor eliminates the need for an external resistor. It provides negative feedback and sets the mid-supply bias point for the inverter.

The board supports a supply voltage of 0.8 to 3.6 V. When the $\overline{\text{EN}}$ input is not in use, it can be driven HIGH, pulling up the X1 input and putting the device in a low-power disable mode. Schmitt trigger action at the $\overline{\text{EN}}$ input lets the circuit tolerate slower input rise and fall times across the entire V_{CC} range.

The 74AUP1Z04 is fully specified for partial power-down applications using I_{OFF} at output Y. The I_{OFF} circuitry disables the output Y, preventing backflow current from damaging the device when it is powered down.

Demonstrate a low-power X-tal driver for crystal oscillator applications

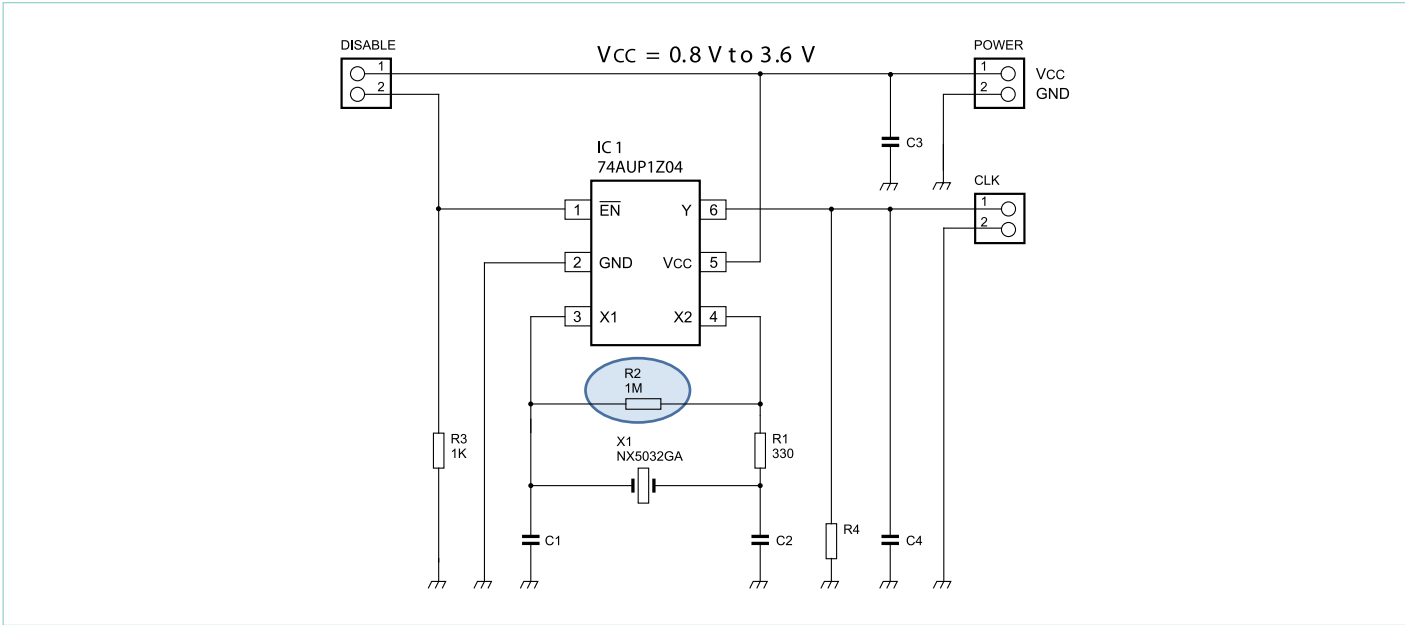
The values of C1 and C2 are calculated so that a parallel combination of C1 and C2 is equal to the recommended load capacitance of the crystal (C_L), as specified in the crystal data sheet. A crystal with a range of frequencies can be used on the board without changing C1 and C2, as long as the load capacitance and footprint are the same. The reference board uses the NDK NX5032GA, a 25 MHz crystal with a load capacitance of 8 pF and a footprint of 5 mm x 3.2 mm. An alternate version of the NX5032GA, with the same footprint and capacitance but a range of 8 MHz to 25 MHz, is also available.

$$C_L = \frac{C1 \times C2}{(C1 + C2)}$$

To obtain a clean waveform, R1 isolates the output of the inverter from the crystal and prevents spurious high-frequency oscillation. The optimum value of R1 depends on the frequency of operation and the required stability. The minimum value of R1 depends on the recommended power consumption of the crystal. Crystal manufacturers usually specify a recommended R1 value in the data sheet. Using an R1 value lower than the

one specified in the data sheet can cause overdriving of the crystal and could result in crystal damage or a shorter crystal life. Acceptable results can be achieved with an R1 value approximately equal to the capacitive reactance (R1 = X_{C2}), provided X_{C2} is greater than or equal to the manufacturer's recommended value.

C2 combines with R1 to form a low-pass filter. The value of C2 can be adjusted according to the desired cutoff frequency and start-up time. In a low-gain amplifier, C2 can be increased over C1 to increase the phase-shift and help in start-up, but C1 needs to be set such that the load capacitance introduced to the crystal does not exceed the manufacturer's recommended value of CL. The values of R4 and C4 can be adjusted to test how different loads effect the edge rates and the shape of the output clock. The $\overline{\text{EN}}$ pin is normally pulled down by R3, when the DISABLE jumper is open. When the DISABLE jumper is closed, the $\overline{\text{EN}}$ pin is pulled up to V_{CC} and the clock output is turned off. The value of R3 can be increased or decreased to control the enable and disable times of the output clock. With a lower R3, the clock can be enabled or disabled faster.



NNP: Normally Not Populated.

Circuit schematic of AUP1Z04 demo board

Test results

Figure 1 shows the output of a 25 MHz crystal at a supply voltage of 3.3 V. Figure 2 shows the output at pin Y when the clock is enabled (that is, when the DISABLE jumper is open). Figure 3 shows the output waveform at a 1.8 V supply, when the clock is enabled. The load used for testing is $R4 = 1\text{ M}\Omega$



Figure 1

and $C4 = 6\text{ pF}$. The sinusoidal waveform of the crystal is converted into a square wave by using the buffered inverter channel of the AUP1Z04. Figure 4 shows the output when the clock is disabled (that is, when the DISABLE jumper is closed and the $\overline{\text{EN}}$ pin is pulled up to V_{CC}).

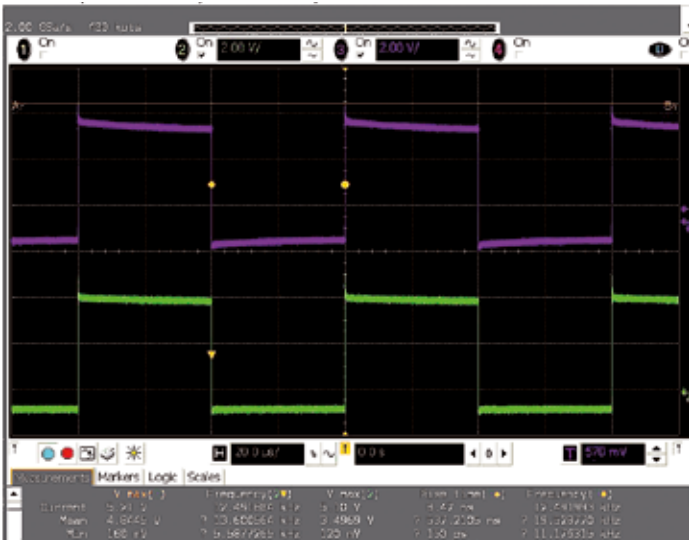


Figure 2

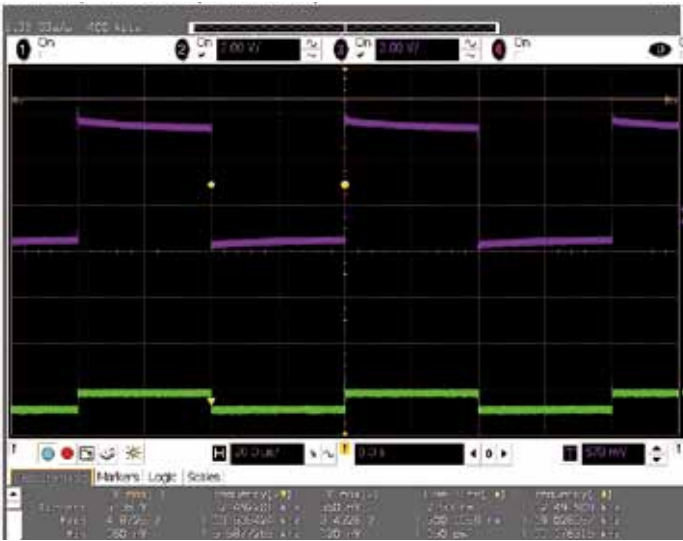


Figure 3

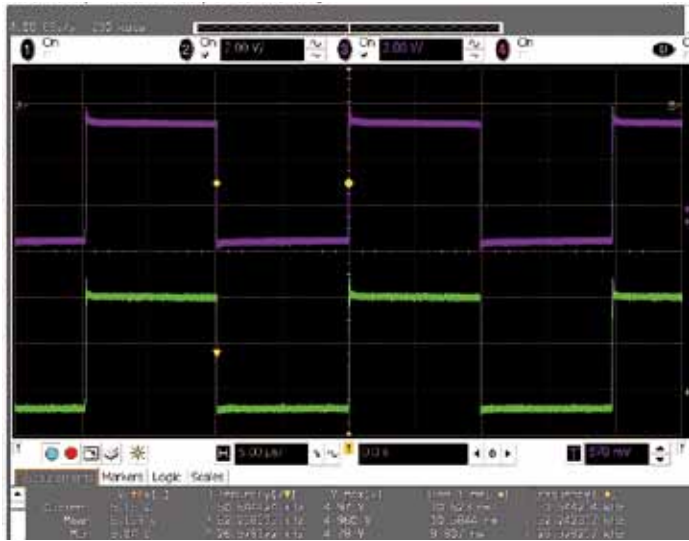

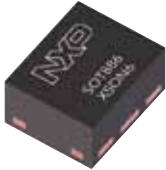



Figure 4

Packages

The 74AUP1Z04 is available in 6-pin SC88 and leadless XSON packages.

Package suffix	GW	GM	GF
			
	SOT363	SOT886	SOT891
	6-pin	6-pin	6-pin
Width (mm)	2.1	1	1
Length (mm)	2	1.45	1
Pitch (mm)	0.65	0.5	0.35

Ordering information

Part number	Package				
	Temp. range	Name	Type	Marking	Material
74AUP1Z04GW	-40 to 125 °C	SC-88	Surface mount	a4	Plastic
74AUP1Z04GM	-40 to 125 °C	XSON6	Thin small outline; no leads	a4	Plastic
74AUP1Z04GF	-40 to 125 °C	XSON6	Thin small outline; no leads	a4	Plastic



NXP 74LVC169 demo board

Demonstrate a binary counter for high-speed counting applications

Use this compact board to demonstrate the 74LVC169, a binary counter with internal look-ahead carry circuitry for cascading in high-speed counting applications.

Key features and benefits

- ▶ Inputs tolerant to 5 V, for use with 5 V logic and in mixed-voltage (3/5 V) applications
- ▶ Wide supply voltage range: 1.2 to 3.6 V
- ▶ Low-power CMOS for portable applications
- ▶ Direct interface with TTL levels
- ▶ Up/down counting
- ▶ Two count-enable inputs for n-bit cascading
- ▶ Built-in look-ahead carry capability
- ▶ Presets for programmable operation
- ▶ Wide range of extremely small standard and leadless packages
- ▶ Wide operating temperature range (-40 to +125 °C), suitable for industrial and automotive applications

Applications

- ▶ Portable devices
- ▶ Industrial
- ▶ Automotive

The 74LVC169 is a synchronous presettable 4-bit binary counter which features an internal look-ahead carry circuitry for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs (pins Q0 to Q3) change simultaneously with each other when instructed by the count-enable (pins CEP and CET) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock (pin CP) input triggers the four flip-flops on the LOW-to-HIGH transition of the clock.

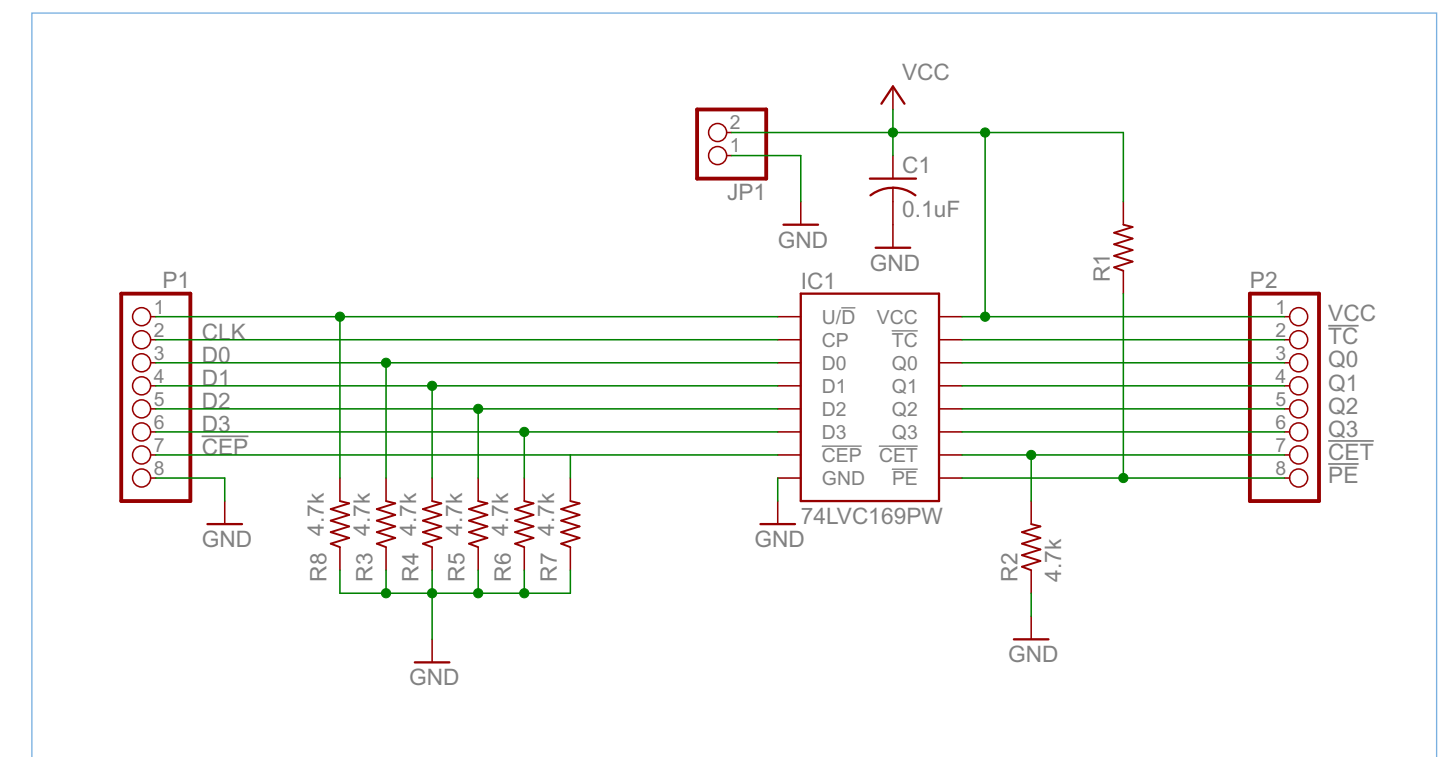
The counter is fully programmable; that is, the outputs may be preset to any number between 0 and its maximum count of 15. Presetting is synchronous with the clock and takes place regardless of the levels of the count enable inputs. A LOW level on the parallel enable (pin PE) input disables the counter and causes the data at the Dn input to be loaded into the counter on the next LOW-to-HIGH transition of the clock. The direction of the counting is controlled by the up/down (pin U/D) input. When pin U/D is HIGH, the counter counts up, when LOW, it counts down.

The look-ahead carry circuitry is provided for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable (pins CEP and CET) inputs and a terminal count (pin TC) output. Both count-enable (pins CEP and CET) inputs must be LOW to count. Input pin CET is fed forward to enable the terminal count (pin TC) output. Pin TC thus enabled will produce a LOW-level output pulse with a duration approximately equal to a HIGH level portion of pin Q0 output. The LOW level pin TC pulse is used to enable successive cascaded stages.

Schematics of 74LVC169 demo board are shown in figure below. A supply voltage of 1.2 to 3.6 V can be used for the board. In this design, the 74LVC169 is used as a clock divider that divides the main clock connected to CP pin by 2, 4, 8 and 16. By default, U/D pin is pulled low and PE pin is pulled HIGH, so counter starts counting down, when clock input edge goes from LOW to HIGH.

The main clock, when connected to the CP pin, is divided by 2 and appears at the Q0 output. There is a clock with 1/4 the frequency of the main clock at Q1. Clocks with 1/8 and 1/16 of main frequency are available at Q2 and Q3 output pins respectively.

In order to preset the outputs of the counter to a number between 0 and its maximum count, the PE pin can be pulled LOW by using jumper JP1. Data at Dn inputs can now be loaded to the outputs on next LOW-to-HIGH transition of main clock. Also, U/D pin can be pulled HIGH by providing logic high input at pin 1 of P1 connector to count up instead of counting down. Since CET pin is pulled LOW, when counter reaches terminal count (HHHH in count up mode and LLLL in count down mode), TC output, which is normally HIGH, will go LOW. The low level on TC output can be used to enable successive cascaded devices.



Circuit schematic of 74LVC169 demo board

Test results

Figure 1 shows a main clock of 466 kHz in green at CP input and a divided-by-2 clock output of 233 kHz in purple at Q0 pin. By default \overline{PE} pin is pulled up to V_{CC} and U/\overline{D} pin is pulled down to GND. Figure 2 shows a main clock of 500 kHz in green at CP input. The Q1 output shows a divided-by-4 clock of

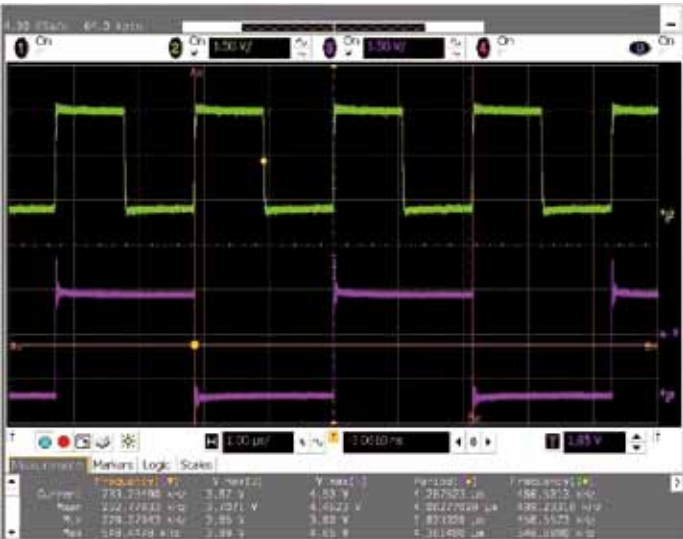


Figure 1

approximately 166 kHz in purple. In this case, U/\overline{D} pin is pulled up so counter starts counting up on rising edge of input clock. Similarly, Figures 3 and 4 show the clock outputs of 71 and 33 kHz, which are approximately 1/8 and 1/16 of main clock respectively. Since U/\overline{D} is pulled LOW for clock output in these examples, counter is counting down.



Figure 2





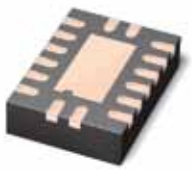

Figure 3



Figure 4

Packages

The 74LVC169 is available in 16-pin SO, SSOP, TSSOP, and leadless DQFN packages.

Package suffix	D	PW	BQ	DS
				
	SOT109-1	SOT403-1	SOT763-1	SOT338-1
	16-pin	16-pin	16-pin	16-pin
Width (mm)	6.0	6.4	2.5	7.75
Length (mm)	9.9	5.0	3.5	6.2
Pitch (mm)	1.27	0.65	0.5	0.65

Ordering information

Part number	Package				
	Temp. range	Name	Type	Marking	Material
74LVC169	-40 to 125 °C	SO16	Small outline	74LVC169D	Plastic
74LVC169DB	-40 to 125 °C	SSOP16	Shrink small outline	LVC169	Plastic
74LVC169PW	-40 to 125 °C	TSSOP16	Thin shrink small outline	LVC169	Plastic
74LVC169BQ	-40 to 125 °C	DHVQFN16	Dual in-line compatible thermal enhanced very thin quad flat package with no leads	LVC169	Plastic

Notes

[illegible]

Notes

[illegible]