AN11196

LPC4300 camera interface design using SGPIO

Rev. 1.1 — 3 December 2012   **Application note**

Revision history

Rev	Date	Description
1.1	20121129	• Editorial changes. • Added pixel clock generation details. • Added VGA implementation recommendations.
1	20121121	• Initial version.

Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

1. Introduction

Serial GPIO is an advanced digital configurable interface on the LPC43xx series microcontroller family from NXP. This interface is perfect for emulating serial and parallel communication protocols. This application note utilizes SGPIO's parallel input capability to provide an example of interfacing a video camera at QVGA (320x240) resolution and 30 fps.

A Keil MCB4300 evaluation board is connected to a Toshiba TCM8230MD camera module to exhibit the SGPIO camera interface solution. Other camera modules that provide a byte wide RGB 5:6:5 data can also be used. The MCB4300 on-board external SDRAM is used to store the video frames from the camera. The camera's output is displayed on the MCB4300's LCD, driven by the LPC4300's LCD controller.
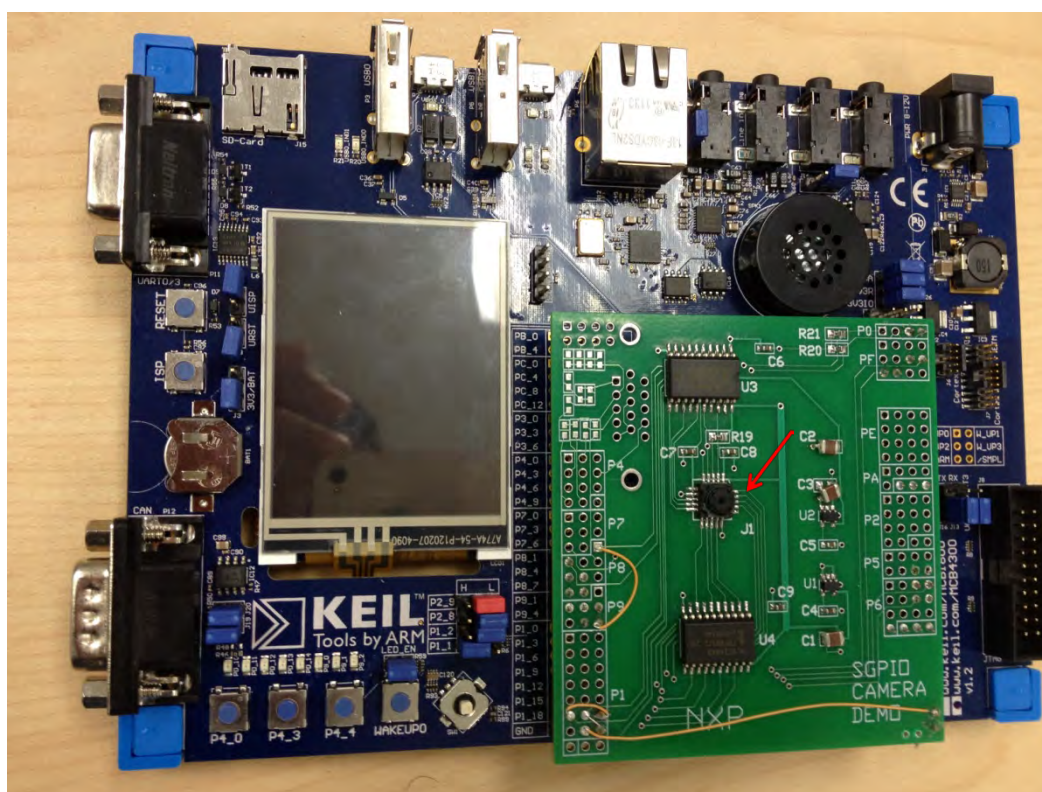

Fig 1.   Camera (red arrow) on interface board

The LPC43xx communicates with the camera's control interface using I²C bus. The Cortex-M4 operates at 180 MHz from PLL1 and this frequency is divided down to generate a 22.5 MHz clock to the CLK3 pin of the LPC4300, which is then sent to the camera for its internal timing.

The TCM8230MD output is a byte wide interface that sends out one byte per pixel clock. This camera output pixel clock is provided to the SGPIO as its slice shift clock. As the camera down samples its VGA signal to output a QVGA signal, the pixel clock frequency needed for the QVGA mode is 22.5/4 = 5.625 MHz with 16 bits per pixel clock. However as the camera output data bus is 8 bits wide, it takes two pixel clocks to output one pixel

AN11196

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

Application note

Rev. 1.1 — 3 December 2012

3 of 13

of image, therefore the pixel clock from the camera to the SGPIO is (22.5/4)*2 = 11.25 MHz, which is half of the camera's input clock frequency. The camera also sends the horizontal and vertical sync pulses which determine the position of the pixel. Fig 2 depicts the signals sent out from the camera to the SGPIO interface.
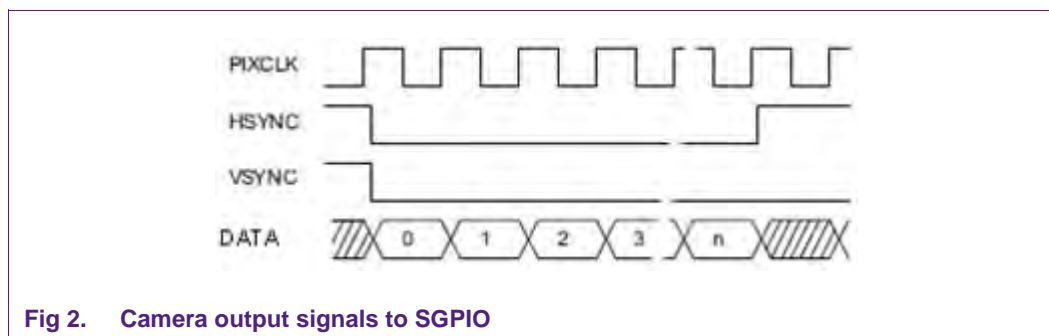

Fig 2.   Camera output signals to SGPIO

2.   Camera SGPIO interface design

The SGPIO interface is made up of 16 slices. Each slice has a 32-bit shift register (slice data register), a 32-bit shadow register (slice data shadow), an internal shift clock (generated from SGPIO_CLOCK) and a position counter (POS) to control the number of bits shifted in or out.

While the SGPIO has some registers for configuration, most designs use a portion of the registers based on the particular application.

The basic building block of SGPIO is a 32-bit slice, organized as a shift register that can shift data 1, 2, 4 or 8 bits at a time. These shift registers can be concatenated together in strings of 1, 2, 4 or 8 words. When all the words are used, the whole group is swapped with their set of shadow registers that have the copy of the next data for output, or acts as a buffer for data on input.

Shifting can be done from an external clock, as in this application, or from an internally generated clock with SGPIO_CLOCK through a prescaler.

Four types of interrupt events are available on the SGPIO interface:

1. Shift clock interrupt

2. Input bit match interrupt

3. Data match interrupt

4. Data capture clock interrupt.

The data capture clock interrupt happens when the POS counter drops to zero and the data register and its shadow register swap their contents. The data capture clock interrupt is used in this example to collect the camera data.

While not used here, the outputs can be enabled by the contents of a slice. Also not used in these examples: a data pattern shifted in can generate an interrupt when it matches a predetermined value. This can be used for address recognition for I²C or SPI slaves.

2.1   SGPIO slices and SGPIO pins used in the camera interface

As shown in Fig 2, different SGPIO pins are assigned to take care of the different input signals from the camera.

As the data bus is byte width, an 8-bit parallel input bus from the SGPIO is needed for the data input from the camera. As the data input is gated by the pixel clock, the pixel clock from the camera is used as the shift clock for the data input.

In this example, 8 slices are concatenated to create a data buffer of 256 bits. Using the 8-bit wide data line, all 8 slices are configured in parallel input byte lane mode. Since each pixel consists of 16 bits, the 8 slices can hold 16 pixels. This means 16 pixels can be handled by the SGPIO interface before the processor has to deal with the data, giving the CPU more time to copy data into SDRAM and to manage other tasks.

Since only SGPIO [11:8] can work as external shift clock, they cannot be used in the 8 slice concatenation group. Therefore, the only choice in this design for the 8 slice concatenation is SGPIO [7:0]. SGPIO8 is chosen as the input shift clock for the 8 concatenated slices. As only SGPIO [11:8] can work as shift clock qualifier input, the horizontal sync pulse taken in from SGPIO9 is used as a slice to qualify the pixel (shift) clock on SGPIO8.

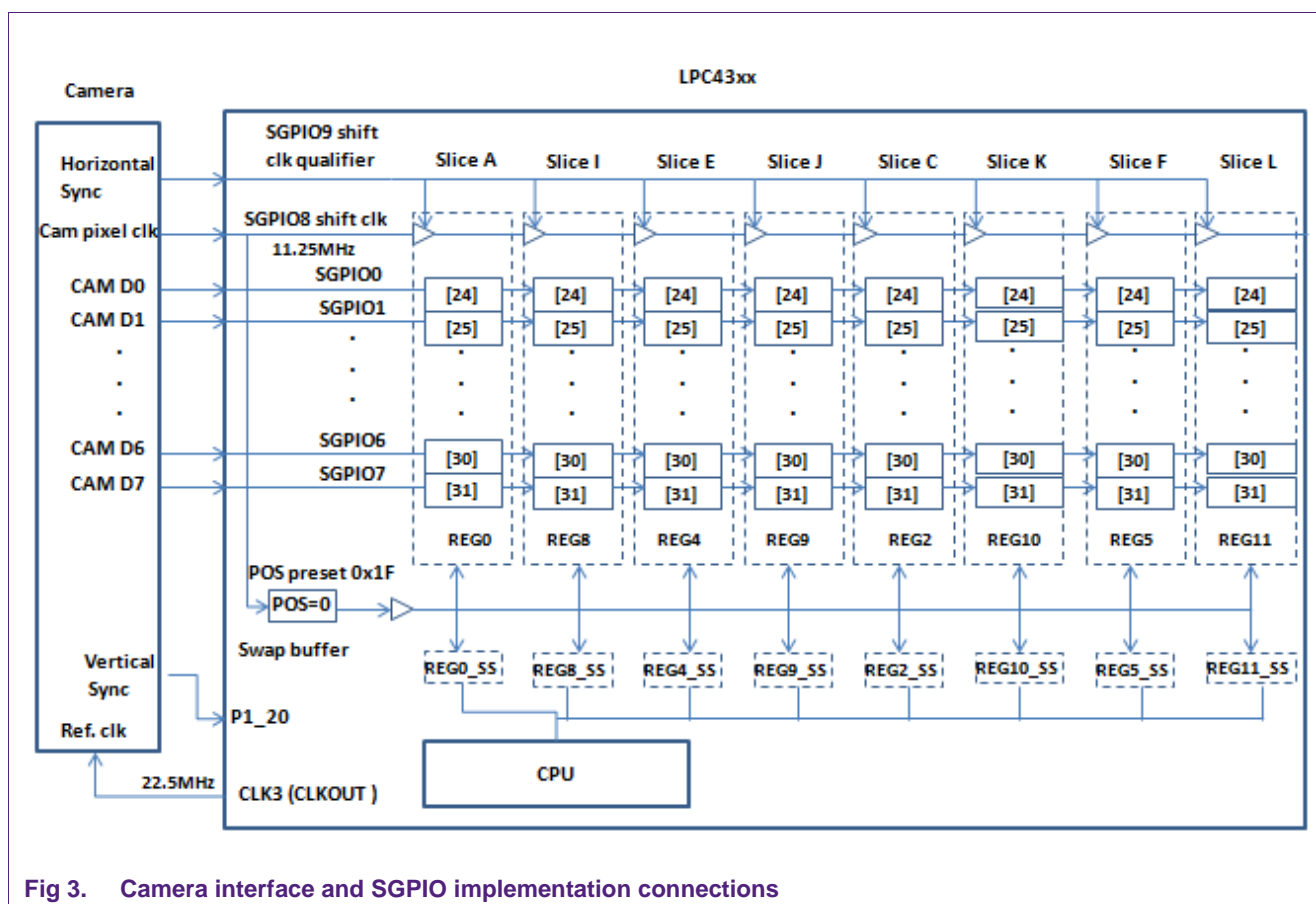The above analysis resulted in the following SGPIO slice and pin selection shown in Fig 3.

Fig 3.   **Camera interface and SGPIO implementation connections**

The Physical SGPIO pin connections with the camera interface are shown in Fig 4:

AN11196

Application note   **Rev. 1.1 — 3 December 2012**   **5 of 13**

LPC4357 pin	SGPIO pins	SGPIO slice	Camera Signals
P9_0	SGPIO0	slice A	Camera Data
P9_1	SGPIO1	slice I	Camera Data
P9_2	SGPIO2	slice E	Camera Data
P9_5	SGPIO3	slice J	Camera Data
P6_3	SGPIO4	slice C	Camera Data
P6_6	SGPIO5	slice K	Camera Data
PF_7	SGPIO6	slice F	Camera Data
PF_8	SGPIO7	slice L	Camera Data
P9_6	SGPIO8	slice B	pixel clock
P8_1	SGPIO9	slice M	horizontal sync, pixel qualifier
P1_20	GPIO0[15]		vertical sync
P1_17			Camera Reset
SCL			SCL
SDA			SDA

Fig 4.   SGPIO pin connections

2.2 Memory allocation for video buffering

A VGA frame requires 640x480 pixels. Each pixel is 16 bits and packed into 32-bit words in the slice buffers. Hence, for VGA format, 640x480/2=153,600 32-bit memory locations are needed to store one frame. These frames can be stored in external SDRAM on the MCB4300 board.

One QVGA frame requires 320x240 pixels. Each pixel is 16 bits and packed into 32-bit words in the slice buffers. Hence, for QVGA format, 320x240/2=38,400 32-bit memory locations are needed to store one frame. These frames are stored in external SDRAM on the MCB4300 board.

AN11196

Application note **Rev. 1.1 — 3 December 2012** **6 of 13**

2.3 Configuring SGPIO slices for QVGA at 30 fps

The steps to setup SGPIO for camera input are shown below. The SGPIOs are inputs using 8 slices to buffer 16 pixels, and data is qualified by the camera horizontal sync.

```
1     turn off all the counters
2     LPC_SGPIO->CTRL_ENABLED = 0;
3
4     All 8 data slices use pixel clock at 11.25 MHz as shift clock
5
6     At each shift clock 8 bits are input
7     LPC_SGPIO->SLICE_MUX_CFG[8 slices] = CLKGEN_EXT | BYTE_MODE;
8
9      slice A SGPIO0 takes the 8 bits in
10     LPC_SGPIO->SGPIO_MUX_CFG[0] = SLICE_8 | EXT_CLK_SGPIO8 | EXT_QUAL_SGPIO9 ;
11     other 7 slices buffer bytes
12    LPC_SGPIO->SGPIO_MUX_CFG[7 slices] = CONCAT_SLICES | SLICE_8 | EXT_CLK_SGPIO8 |
      EXT_QUAL_SGPIO9 ;
13
14    8 slice buffer data is available after 32 shift clocks
15    LPC_SGPIO->POS[11] = ((32-1)<<8) | (32-1);
16
17    --------
18
19    now turn on all the slices
20     LPC_SGPIO->CTRL_ENABLED = (8 slices);

          -------
```

2.4 SGPIO receiving and displaying pixel data

In this example, the CPU collects the camera image in the capture data swap interrupt. Initial synchronization is done by the CPU waiting for a Vertical Sync pulse change, which only happens at the start of a frame. Once the vertical sync pulse is detected, the data swap interrupt service routine starts the image data collection process. Every time an exchange data interrupt is reported on slice A, the application collects the 8 slices of new camera data. When one entire frame is collected, the image is then displayed on the LCD.

By utilizing 8 concatenated slices in parallel mode with a 256-bit buffer, the camera video capture for the 30 fps QVGA takes less than 5 % of the CPU's bandwidth at 180 MHz. This leaves the Cortex-M4 with enough bandwidth for more signal processing algorithms. The same implementation can also be achieved with the on-chip Cortex-M0 core. As the image collection interrupt finishes within 0.5 µs, any other application that can tolerate an interrupt about 0.5 µs can share the CPU resource.

The flow chart in Fig 5 shows the software architecture for the video camera frame capture.

AN11196

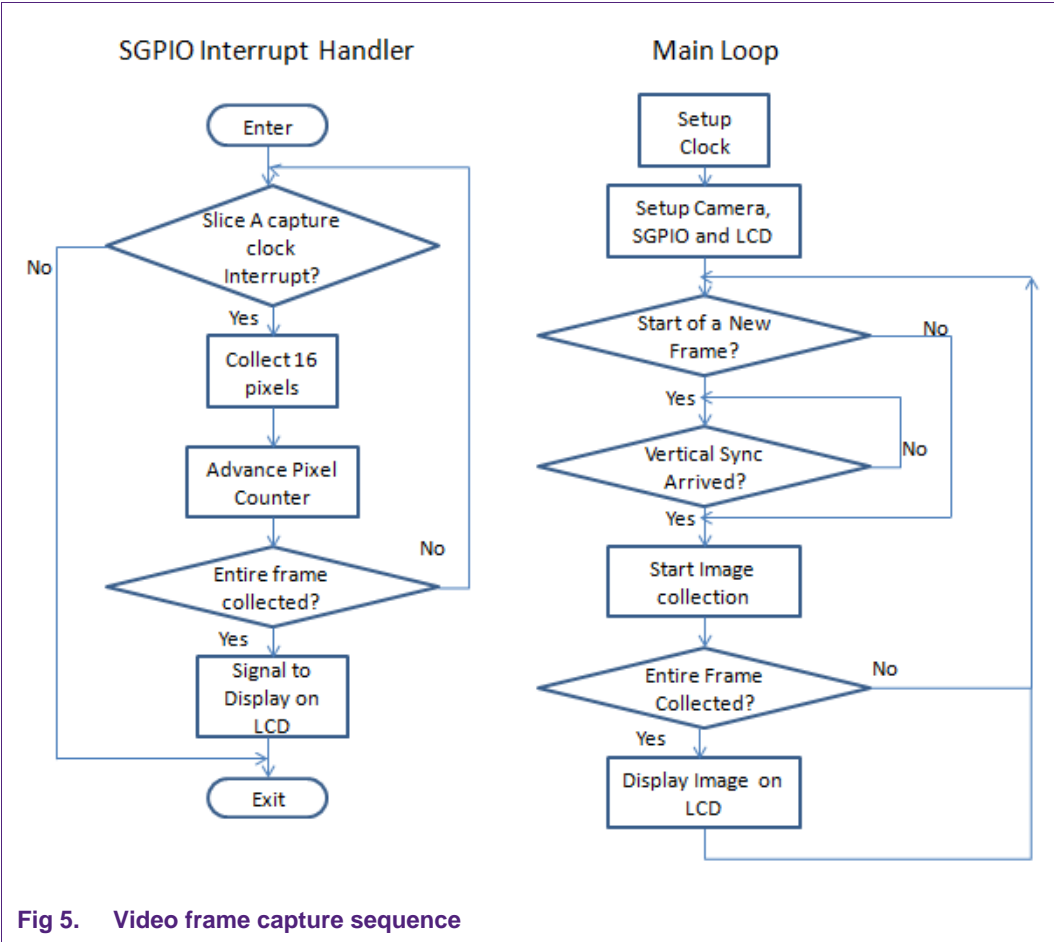**Application note** **Rev. 1.1 — 3 December 2012** **7 of 13**

Fig 5.   Video frame capture sequence

It should be noted that the LCD on this development board is 240x320, but the QVGA from the camera is 320x240. Therefore, every frame is displayed 16 bits a time on the LCD, rearranged to match the LCD pixel positions. This rearrangement action is shown in the above flow chart as action item "Display Image on LCD".
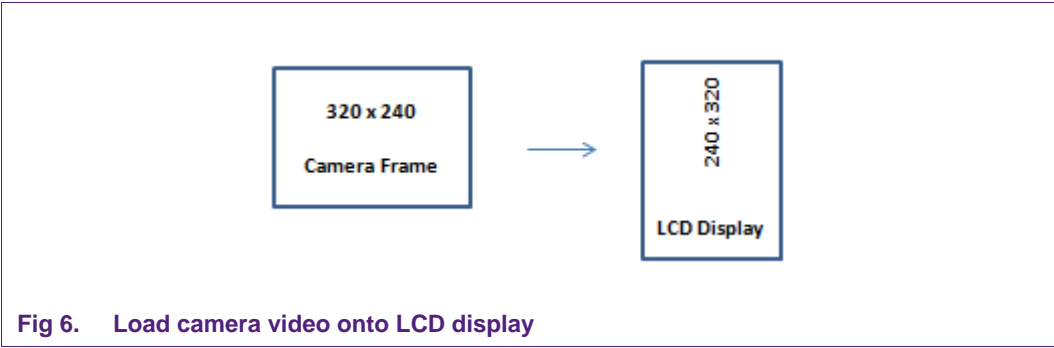

Fig 6.   Load camera video onto LCD display

2.5 Adapt QVGA to VGA format

The following considerations are recommended to adapt from QVGA to VGA format:

1. Configure the camera for VGA format through I²C interface.

2. Control SGPIO camera interface from Cortex-M0 instead of Cortex-M4. The bandwidth usage for VGA format is 4 times of the QVGA format with the current implementation. User can utilize the asymmetric dual core in LPC4300 to offload the camera interface from Cortex-M4 to reserve more DSP processing power.

3. Consider using DMA to transfer image data from SGPIO to memory. This will reduce the CPU bandwidth usage of the camera interface.

4. Handle down sampling or do windowing to display on QVGA format LCD.

3. Conclusion

The LPC4300 series microcontrollers feature a rich set of NXP unique advanced peripherals including the digitally configurable interface SCT and SGPIO. With SGPIO's capability in slice/buffer concatenation and its flexibility in clock and interrupt control, the SGPIO interface is a perfect candidate for parallel interface design like the camera interface. These key advantages allow users to take care of some of the otherwise CPU intensive applications with concise implementation and very little CPU involvement, leaving the CPU with more bandwidth to build up the ever increasingly complicated application system.

4. Appendix

Fig 7.   Camera to SGPIO schematic
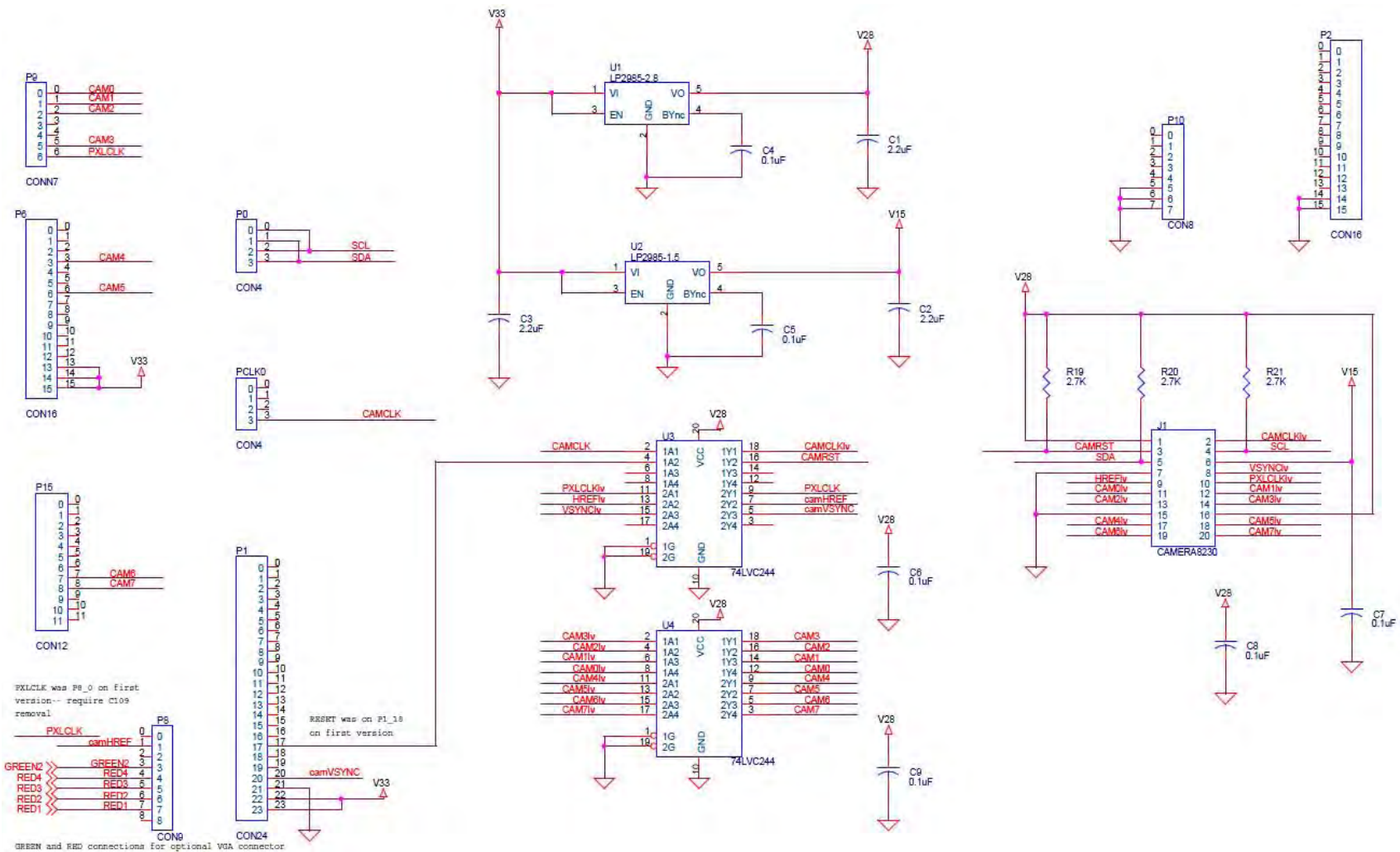
5. Legal information

5.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

5.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP

Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

5.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are property of their respective owners.

6. List of figures

7. Contents