AN11248

In-System Programming of LPC18xx/43xx flash

Rev. 1 — 9 August 2012 Application note

Document information

Info	Content
Keywords	ISP, In-System Programming, MCB4300, Flash Magic, Blinky, LPC18xx, LPC43xx, LPC4357, µVision 4
Abstract	Programming flash using In-System programming with Flash Magic

Revision history

Rev	Date	Description
1	20120809	Initial version.

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1. Introduction

This application note provides an overview of In-System programming (ISP) and easy steps to program the on-chip flash of LPC18xx/43xx flash based Cortex M3/Cortex M4 microcontrollers using Flash Magic software. Keil's MCB4300 evaluation board is used for demonstration purposes.

LPC18xx/43xx flash-based chips contain up to 1 MB flash divided into two banks:

- Bank A: `0x1A00 0000` (512 KB max.)
- Bank B: `0x1B00 0000` (512 MB max.)

In an LPC18xx/43xx with on-chip flash, USART0 or USART3 can be used for ISP communication depending on the OTP bits and/or boot pins. If all boot pins are held low, USART0 is selected.

2. In-System Programming

In-system programming (ISP) via USART0 is used for this demo with the following pin configuration:

- P2_0 FUNCTION 1, USART0 TXD
- P2_1 FUNCTION 1, USART0 RXD

ISP mode can be entered using pin P2_7 pulled low (GND) before RESET. This pin is controlled via the 'ISP' button on an MCB4300/MCB1800 board.

2.1 Requirements

The following items are used for demo of this application note:

- Keil MCB4300/MCB1800 evaluation board
- Keil MDK for ARM (v.4.50 or higher), evaluation version is sufficient
- RS232 serial cable
- Optional USB-to-serial adapter, in case a standard serial port is not available on PC
- Flash Magic software (version 6.8 or higher) – it can be downloaded for free from Embedded Systems Academy http://www.flashmagictool.com/
- Micro USB cable supplied with MCB4300 board or 6 V to 12 V power adapter with at least 500 mA output current.
- Optional RS232 terminal software, e.g. Terminal v1.9b

Note: It is assumed that all items mentioned above are in place and necessary drivers are already installed.

2.2 Blinky sample code

The example code ‘Blinky’ is used for this demo. Open Keil µVision 4 and browse the Blinky project for MCB4300 board at following location:

`C:\Keil\ARM\Boards\Keil\MCB4300\Blinky\Blinky.uvproj`

There are three target options defined in this project:

- LPC4350 RAM (default)
- LPC4350 external flash
- LPC4350 SPIFI

All three target options are available from the ‘Select Target’ drop-down menu.

An additional target option needs to be added for ‘LPC4350 Flash Bank A’:

- Right click on ‘LPC4350 RAM’ root directory from ‘Project’ explorer window and select ‘Manage Components…’ option from pop-up menu as shown in Fig 1.

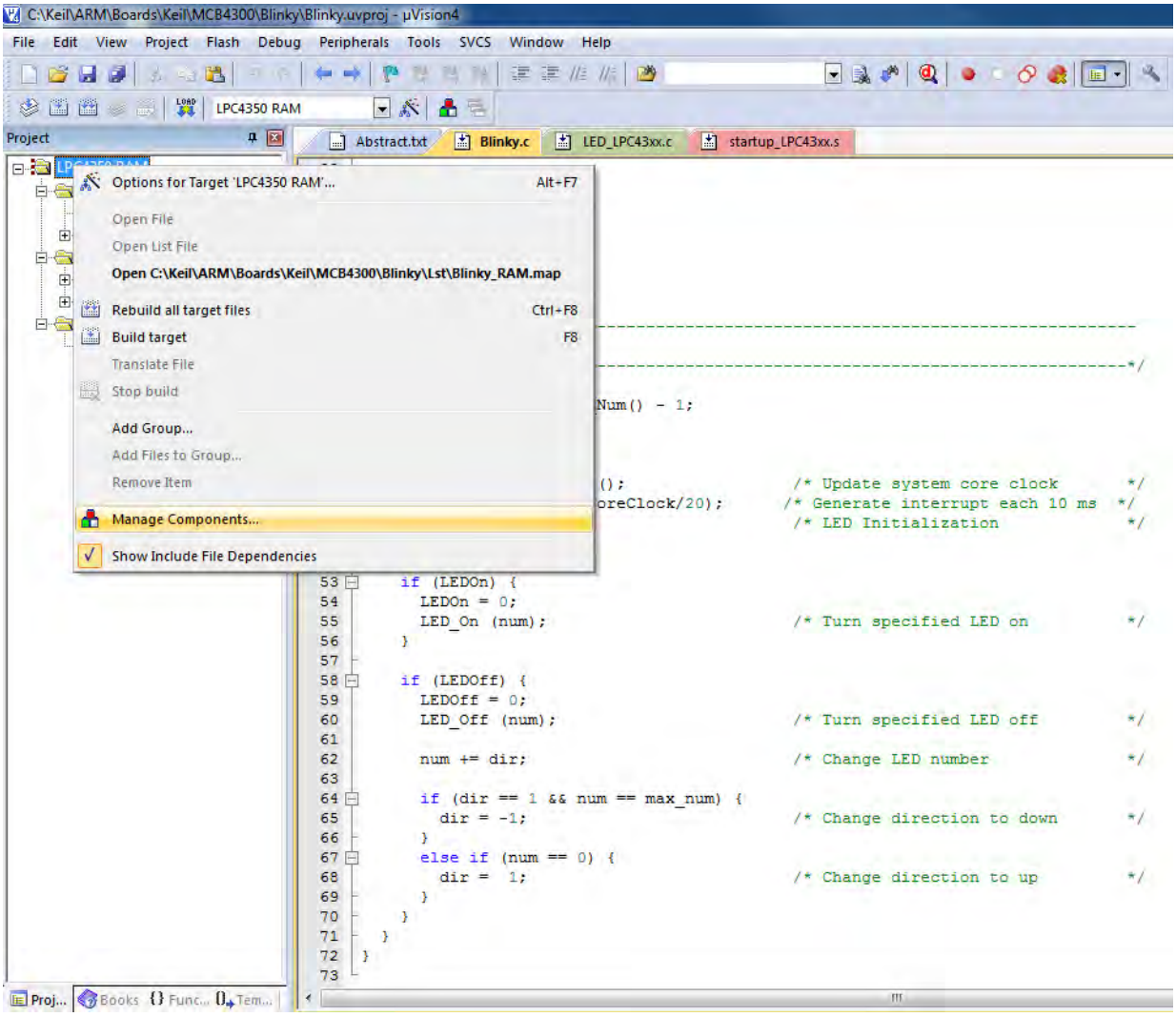

Fig 1. Blinky project in Keil uVision 4 showing Target options menu

- Components, Environment and Books window pops up with Project Components tab active. In Project Targets option, click New (Insert) button , type ‘LPC4350 Flash Bank A’ and press Enter. It is added into Target option list as shown in Fig 2. Click OK when done.

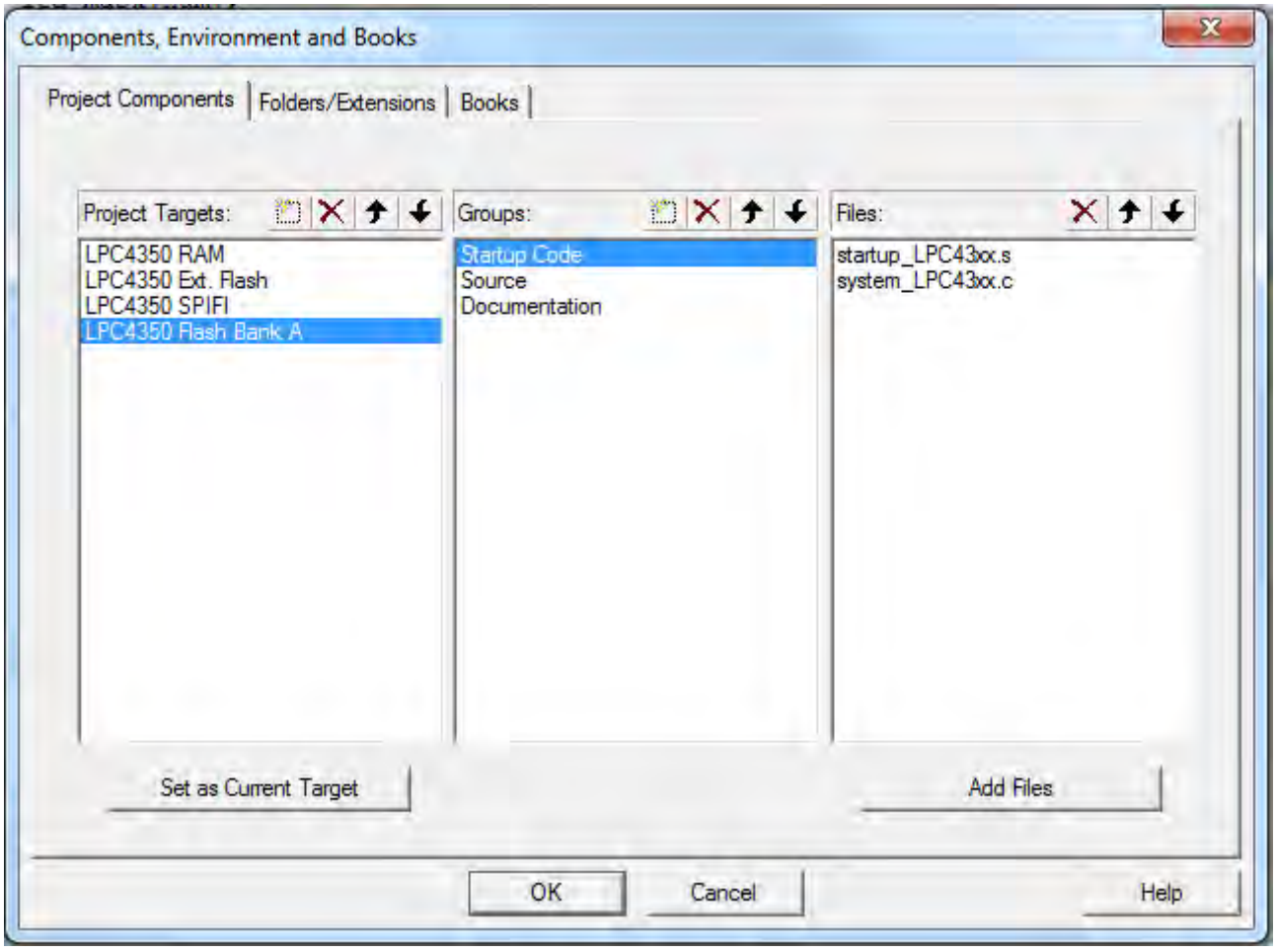

Fig 2. Managed Components window

- Select ‘LPC4350 Flash Bank A’ from Select Target drop-down menu and click Target Options button next to it; ‘Options for Target LPC4350 Flash Bank A’ window pops up with ‘Target’ tab active. Select internal ROM address as 0x1A000000 with size 0x4000; it is sufficient for this demo. Leave the RAM address as-is; the rest of the settings will remain the same as shown in Fig 3.

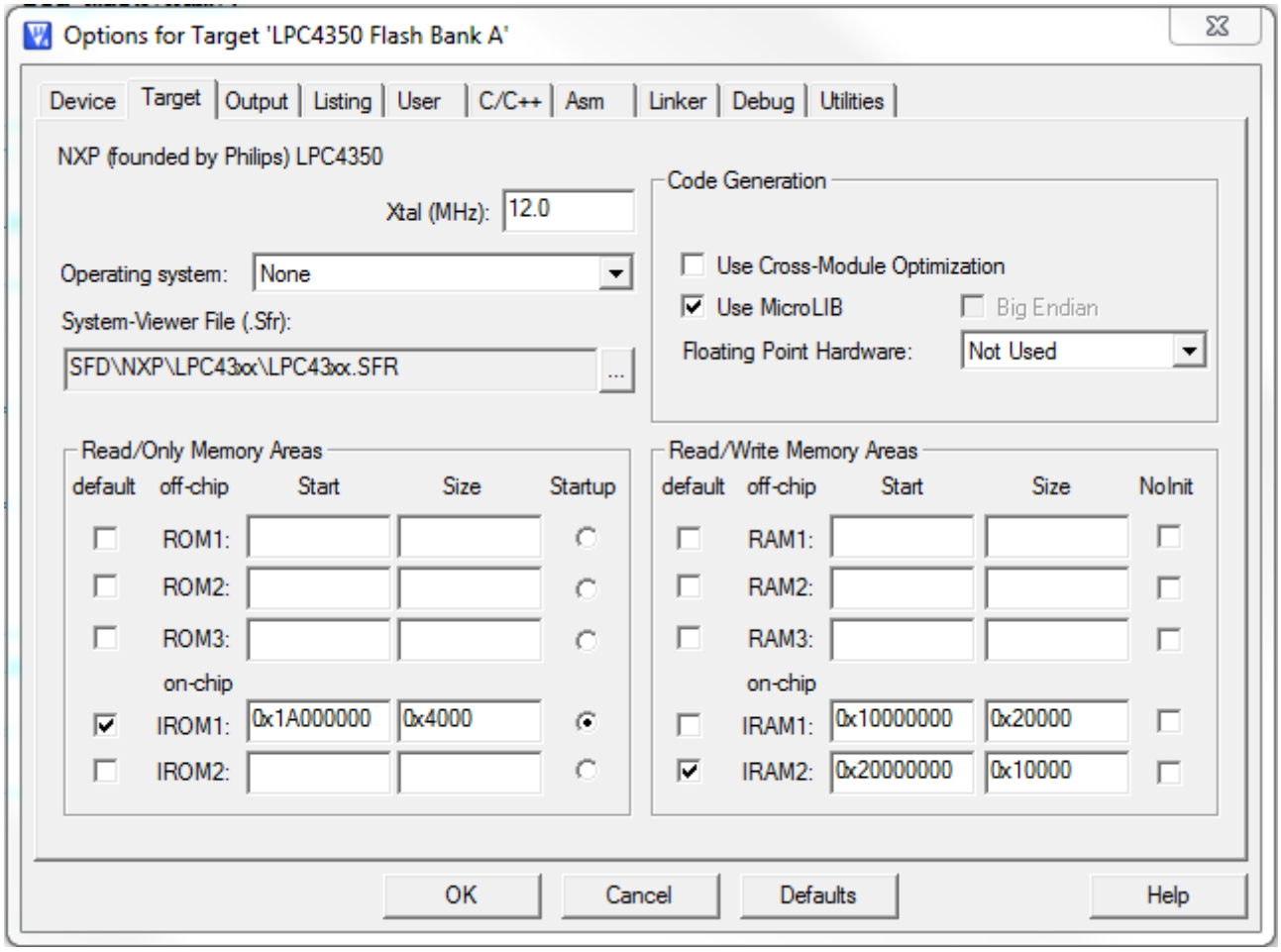

Fig 3. Options for Target Window – Target Tab

- Click ‘Output’ tab and change the name of the executable to ‘Blinky_Flash_Bank_A’. Also check the ‘Create HEX file’ option as shown in Fig 4. The compiler will generate ‘Blinky_Flash_Bank_A.hex’ file into default ‘Obj’ folder. This file will be used for programming flash using ISP. Click OK when done.

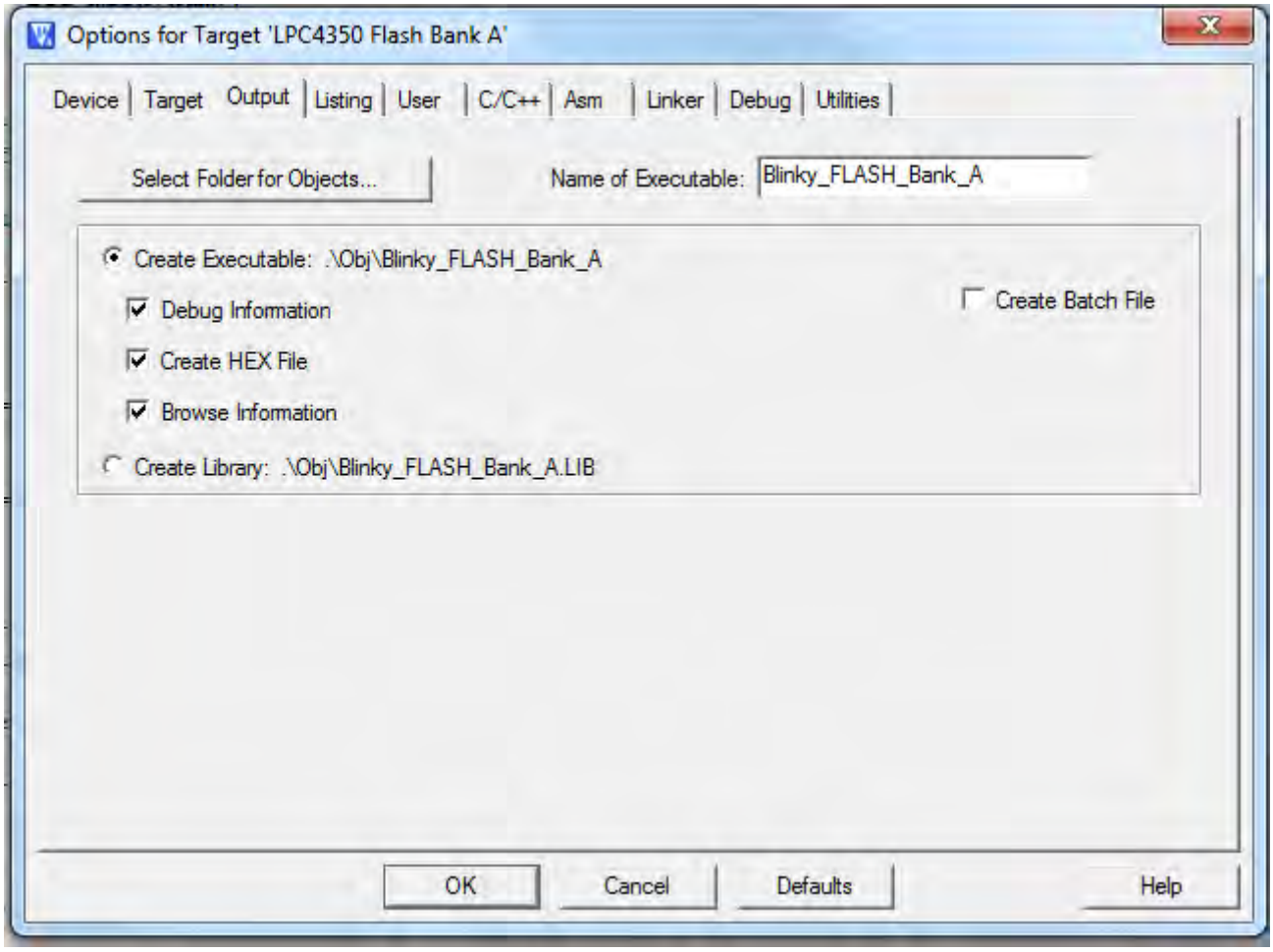

Fig 4. Options for Target Window – Output tab

- Click ‘Rebuild’ button to compile the project with ‘LPC4350_Flash_Bank_A’ target selected. Check if the ‘Blinky_FLASH_Bank_A.hex’ file is created in the ‘Obj’ folder.

A target project for ‘LPC4350_Flash_Bank_A’ and its .hex file has now been successfully created. The next step is to program the internal flash with the newly created .hex file.

2.3 Steps for In-System Programming using Flash Magic

Keil's MCB4300 is selected for this demo with an LPC4357 chip placed on it. This chip has 1 MB on-chip flash, and we are going to program its bank0 at address `0x1A000000`. The MCB4300 evaluation board is shown in Fig 5.

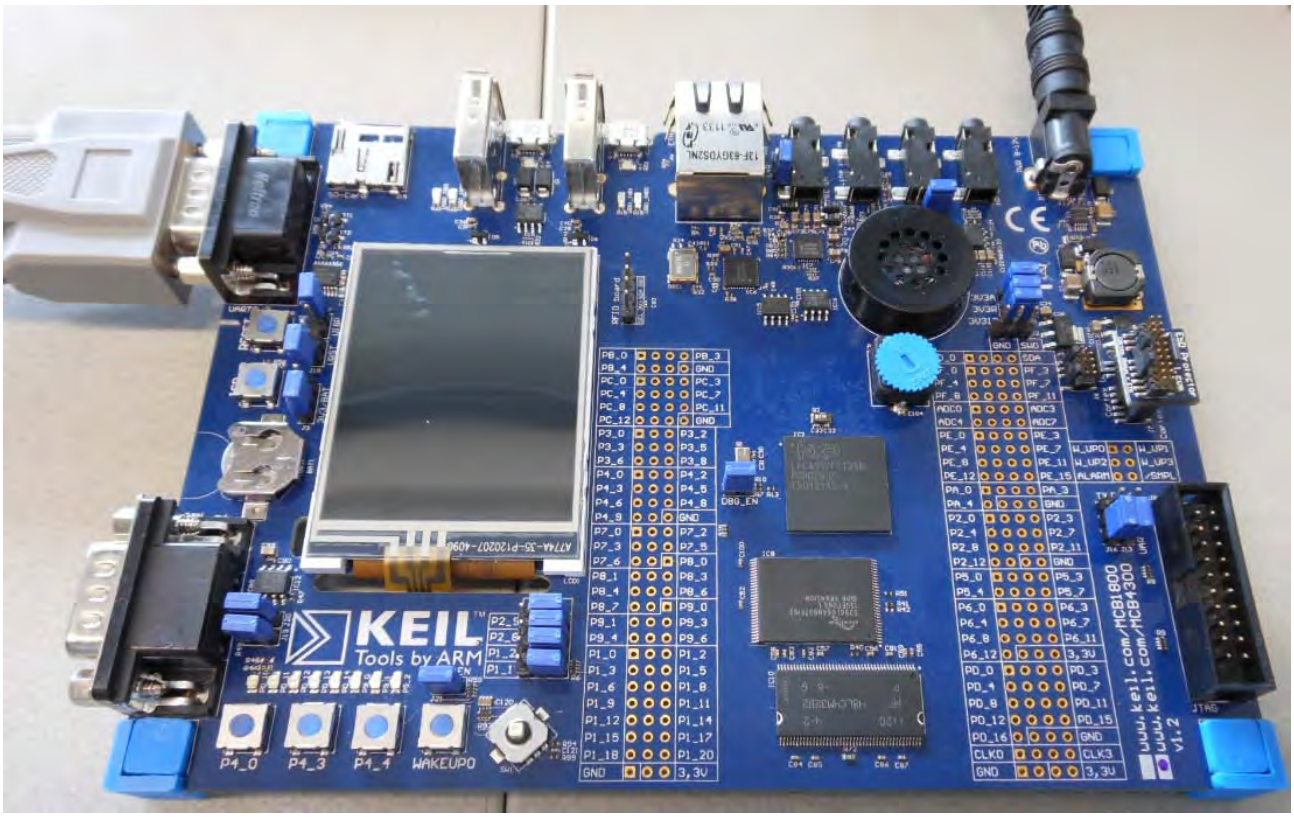

Fig 5. Keil MCB4300 evaluation board

- First, check the jumper settings of the board and make sure the position of jumpers J13 and J16 are set for UART0 as shown in Fig 6 (Top). Boot pins P1_1, P1_2, P2_8 and P2_9 are held low, as shown in Fig 6 (Bottom), so that it can boot from internal flash on RESET after programming. Also, J17 should be open to manually enter ISP mode using the ISP button.

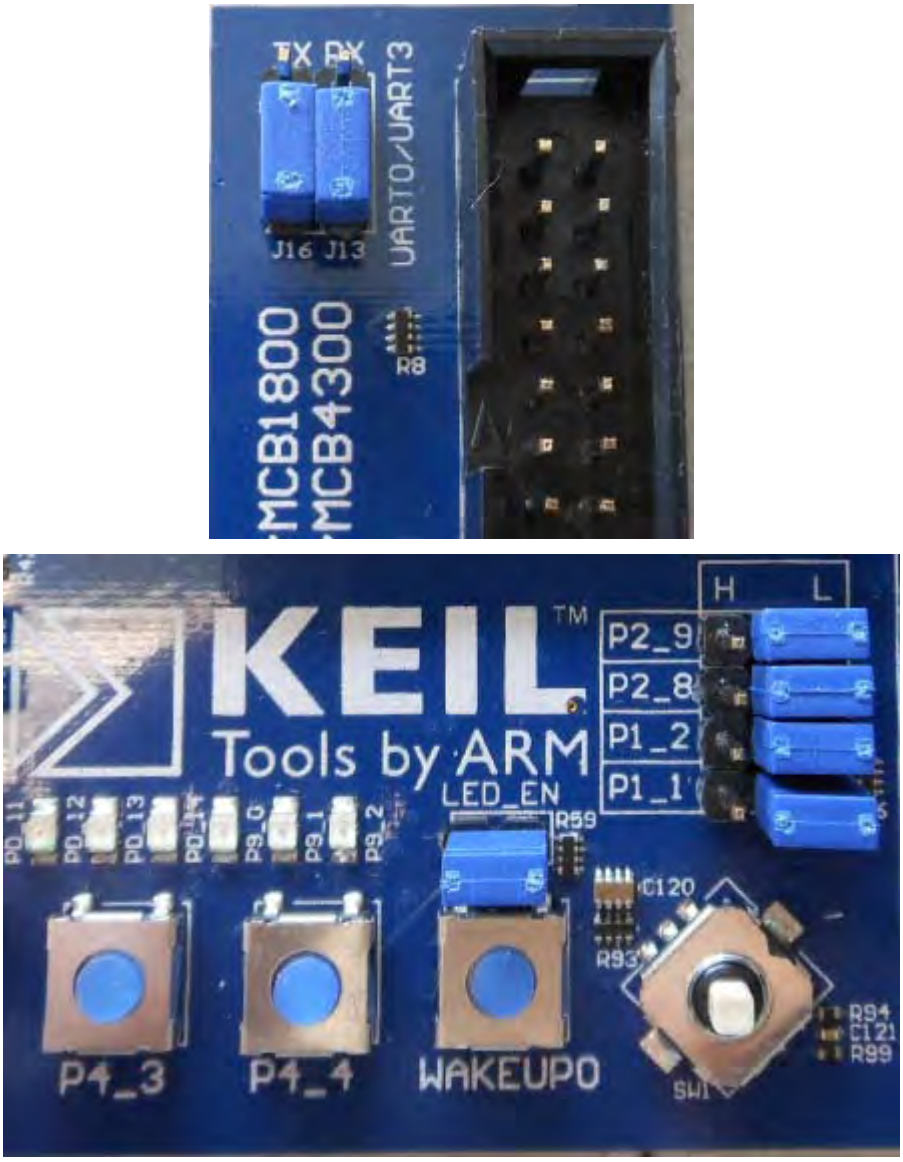

Fig 6. Jumper settings for MCB4300

- Connect the Serial Cable to the DB9 connector on the top left corner named UART0/3, and connect the other end to a PC. Check that the exact COM port associated is known; otherwise, check it from Device Manager in Windows. Also, connect the power adapter into socket P1 and turn ON power, or use a Micro USB cable to power the board from the PC.
- Press and hold ISP button, and then press RESET button; release ISP button after releasing RESET button. The LPC4357 enters ISP mode, which can be easily verified using any terminal software by sending synchronization character '?'; it should respond with message 'Synchronized'.
- Open Flash Magic by clicking the icon on desktop. In Step 1: Click on 'Select' button and select LPC4357, select Bank 0 from 'Flash Bank' drop down menu, select

COM port for your PC, Baud Rate = 9600, Interface = None (ISP) and Oscillator (MHz) = 12. You may also select ‘Erase all Flash’ option in Step 2.

- In Step 3: click ‘Browse’ button and select ‘Blinky_FLASH_Bank_A.hex’ file from the location:
  `C:\Keil\ARM\Boards\Keil\MCB4300\Blinky\Obj\Blinky_Flash_Bank_A.hex`
- In Step 4: select ‘Verify after programming’ and ‘Activate Flash Bank’ options.

These settings are shown in Fig 7.

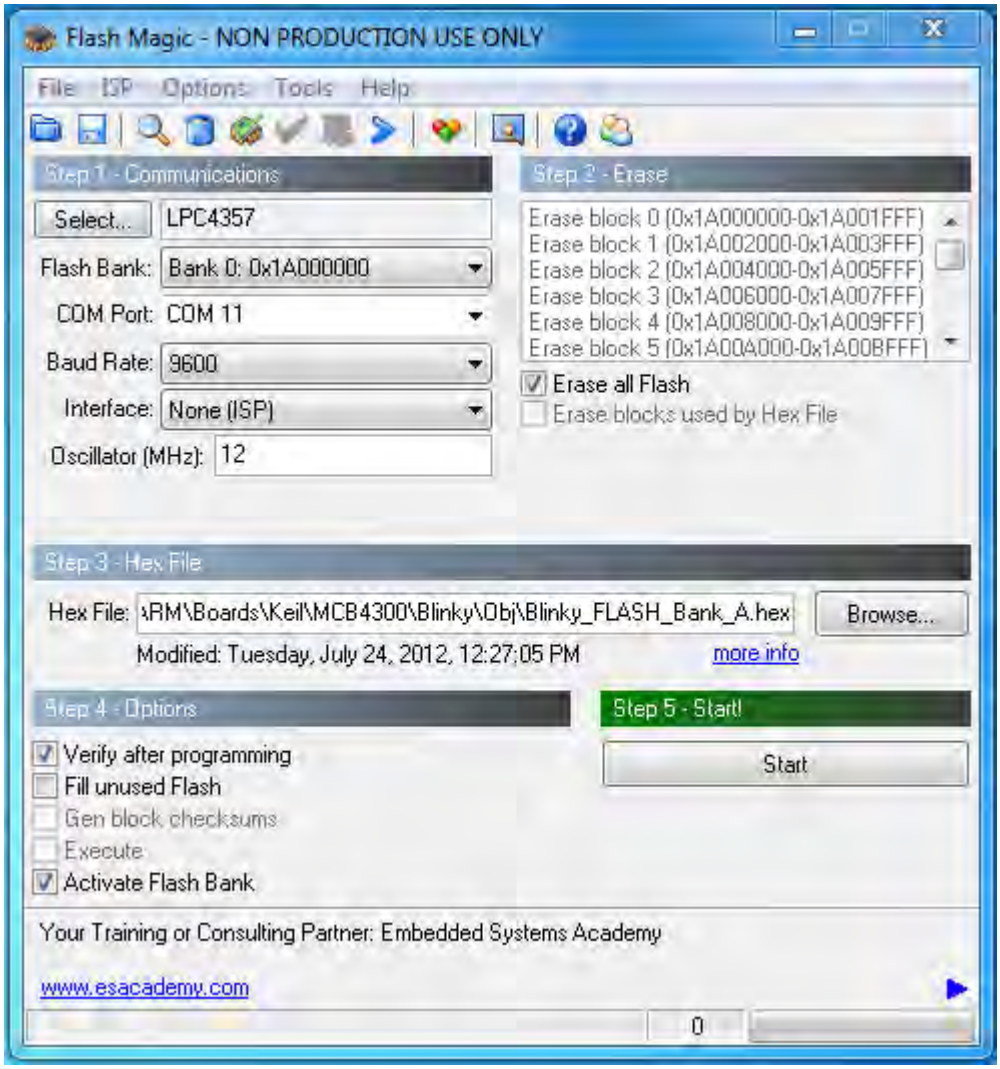

Fig 7. Flash Magic window

- Click ‘Start’ button to start Flash programming. The status bar at the bottom of the Flash Magic window shows the status during programming. When flash programming finishes successfully it shows the message ‘Finished’ in the status bar as shown in Fig 8.

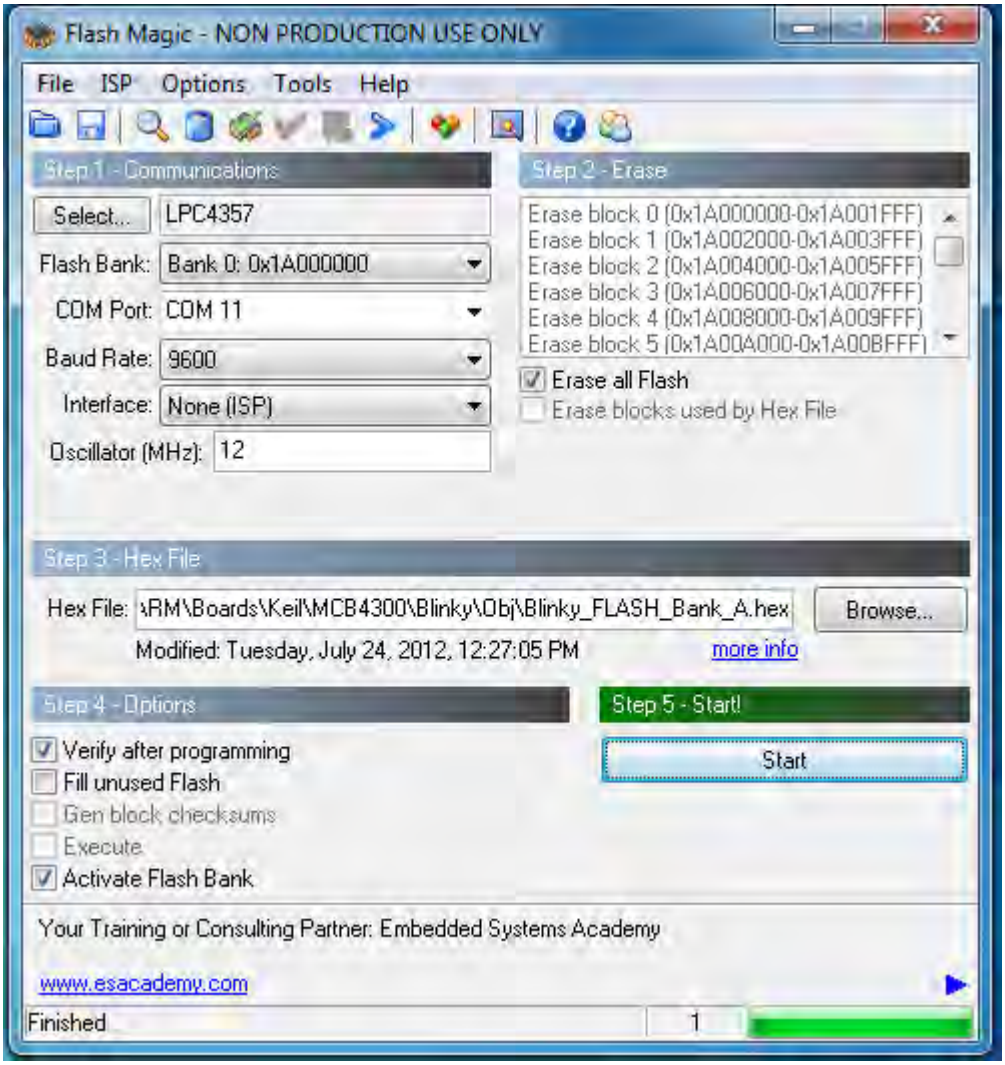

Fig 8. Flash programming done successfully

- Press RESET button to finish ISP mode and boot from internal flash. Now you should see blinking LEDs.

Congratulations! You have successfully programmed the internal flash of LPC4357 chip.

ACTIVITY: Use the steps mentioned in sections 2.2 and 2.3 to create a target project for Flash Bank B.

3. Implications of Code Read Protection (CRP) on flash

Code Read Protection is the mechanism to restrict the access to on-chip flash and ISP. The demo does not use CRP for simplicity – check 'Asm' tab in Target Options. CRP is invoked by programming a specific pattern in flash at 0x2FC. There are four different levels of CRP security defined for LPC18xx/43xx which are defined in Table 1:

Table 1. Code Read Protection options

Name	Pattern programmed in 0x000002FC	Description
CRP1	0x1234 5678	Chip access via JTAG pins is disabled. This mode allows partial flash update using the following ISP commands and restrictions: • Because the ISP code uses SRAM, the Write to RAM command cannot access SRAM below 0x1000 0200 • Read Memory command: disabled. • Copy RAM to flash command: cannot write to Sector 0. • Go command: disabled. • Erase sectors command: can erase any individual sector except sector 0 only, or can erase all sectors at once. • Compare command: disabled This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased. The compare command is disabled, so in the case of partial flash updates the secondary loader should implement a checksum mechanism to verify the Integrity of the flash.
CRP2	0x8765 4321	This is similar to CRP1 with the following additions: • Write to RAM command: disabled. • Copy RAM to Flash: disabled. • Erase command: only allows erase of all sectors.
CRP3	0x4321 8765	This is similar to CRP2, but ISP entry by pulling P2_7 LOW is disabled if a valid user code is present in flash sector 0. This mode effectively disables ISP override using the P2_7 pin. It is up to the user's application to provide for flash updates by using IAP calls or by invoking ISP with UART0. **Caution**: If CRP3 is selected, no future factory testing can be performed on the device.
NO_ISP	0x4E69 7370	Disables ISP request using the P2_7 pin.

Important: Any CRP change becomes effective only after the device has gone through a power cycle.

4. Flash signature

For LPC18xx/LPC43xx parts with on-chip flash, a hardware flash signature generation capability is built into the flash memory. This feature can be used to create a signature that can then be used to verify the flash contents. The generator can produce a 128-bit signature from a range of flash memory. It is located at the reserved exception vector location 7 (offset 0x001C in the vector table). It should contain the 2's complement of the check-sum of table entries 0 trough 6. This causes the checksum of the first 8 table entries to be 0. The boot loader code checksums the first 8 locations in sector 0 of the flash. If the result is 0, then execution control is transferred to the user code.

Now Flash Magic with version 6.80 can force to always put the correct checksum in by checking the option 'Activate Flash Bank' in Step 4 of its main window as shown in Fig 7.

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Date of release: 9 August 2012
Document identifier: AN11248