

AN11024

SDARS active antenna 2nd stage LNA with BFU690, 2.33 GHz

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Application note

Document information

Info	Content
Keywords	LNA, 2.33 GHz, BFU690, SDARS
Abstract	This application note provides circuit, layout, BOM and performance information for 2.33GHz LNA equipped with NXP Semiconductors BFU690 wideband transistor



Revision history

Rev	Date	Description
v.1	20110324	initial version

Contact information

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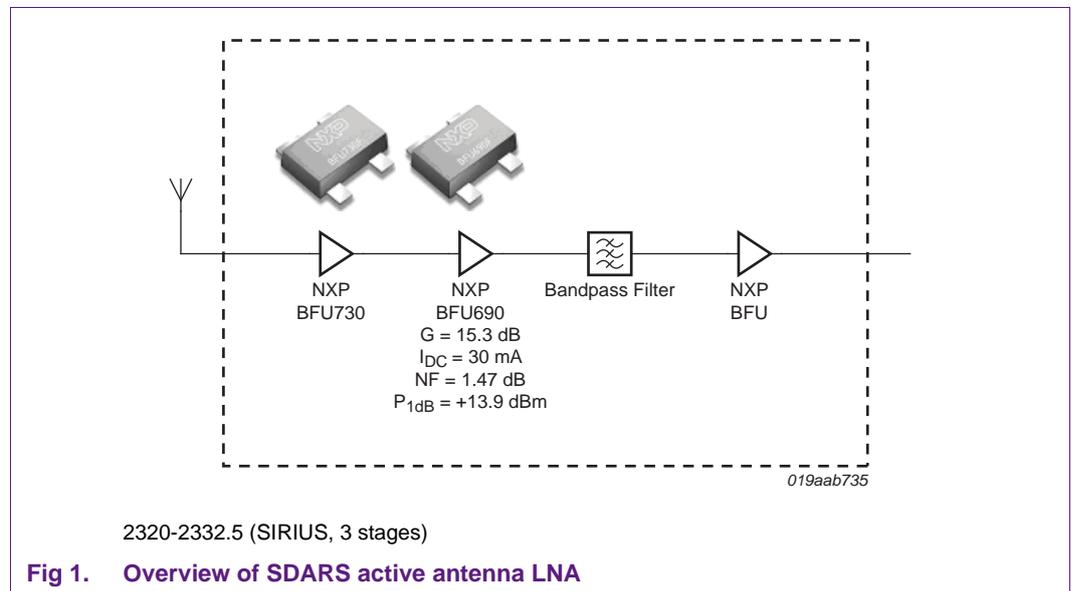
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1. Introduction

The BFU690 is a wideband Silicon Germanium Amplifier transistor intended for high speed, low noise applications. It is designed to be used for LNA applications such as GPS, satellite radio, cordless phone and wireless LAN. The BFU690 comes in a SOT343F package providing 2 emitter pins for better grounding.

The BFU690 is ideal in all kind of applications where cost matters. It also gives the designer flexibility in his design work.

The BFU690 SiGe low noise transistor is shown here in a Satellite Digital Audio Service (SDARS) active antenna LNA application. It is intended for use as the 2nd stage in a 3 stage SIRIUS LNA chain.



The 2.33 GHz LNA evaluation board (EVB) is designed to evaluate the performance of the BFU690 transistor applied as the 2nd stage in a 3 stage SIRIUS LNA chain. In this document, the application diagram, board layout, bill of material, and some typical results are given.

The evaluation board is shown in [Figure 2](#)

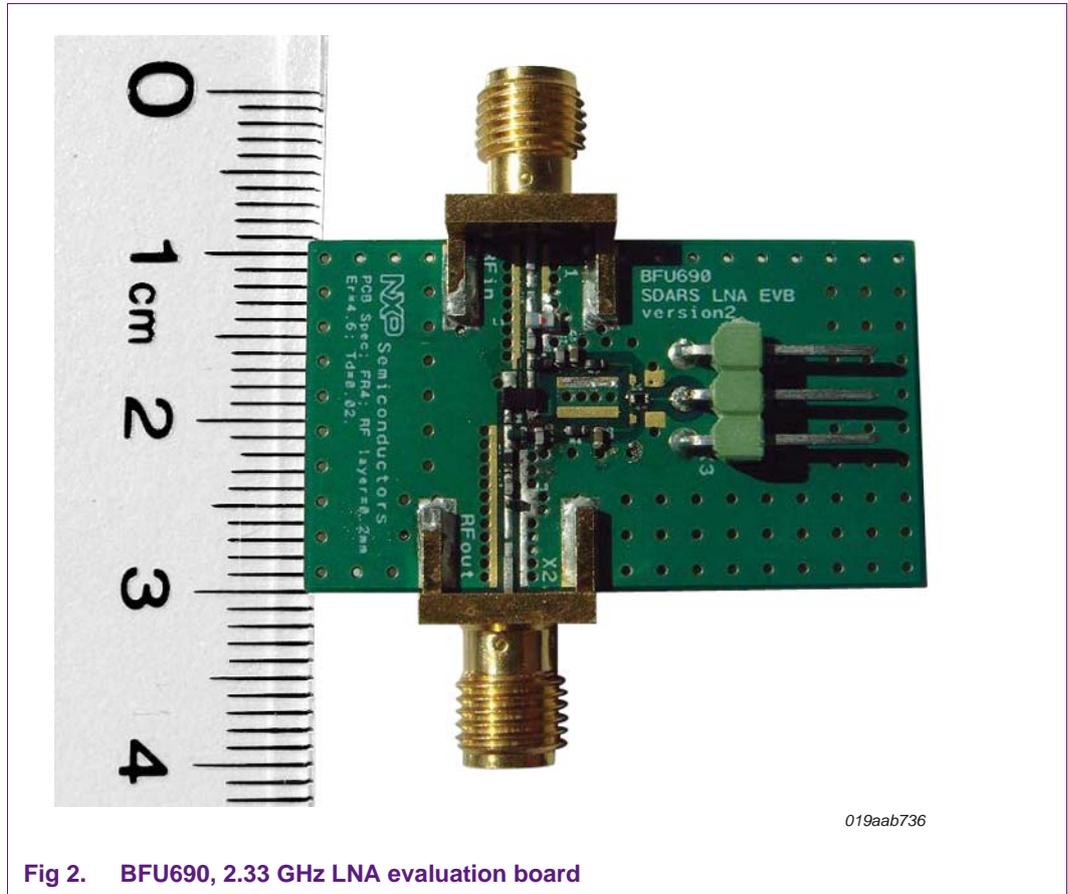


Fig 2. BFU690, 2.33 GHz LNA evaluation board

2. General description

The BFU690 is a NPN silicon germanium microwave transistor for high speed, low noise applications in a plastic, 4-pin dual-emitter SOT343F package. [Table 1](#) shows a summary of the transistor performance in terms of noise and gain.

Table 1. BFU690 performance in terms of noise and gain measured at $V_{CE} = 2\text{ V}$; $I_C = 25\text{ mA}$

Frequency (GHz)	Noise figure (dB)	Associated gain (dB)
1.5	1.13	19.5
2.4	1.51	15.7

Table 2. BFU690 pinning information

Pin	Description	Simplified outline	Graphic symbol
1	emitter		
2	base		
3	emitter		
4	collector		

3. Application board

The BFU690 2.33GHz EVB simplifies the evaluation of the BFU690 wideband transistor, for this frequency range. The EVB enables testing of the device performance and requires no additional support circuitry. The board is fully assembled with the BFU690, including input and output matching, to optimize the performance. The input match was a compromise between the best noise figure and a low input return loss. The board is mounted with signal input and output SMA connectors for connection to RF test equipment:

3.1 Application circuit

The application diagram as supplied on the evaluation board is shown in [Figure 3](#).

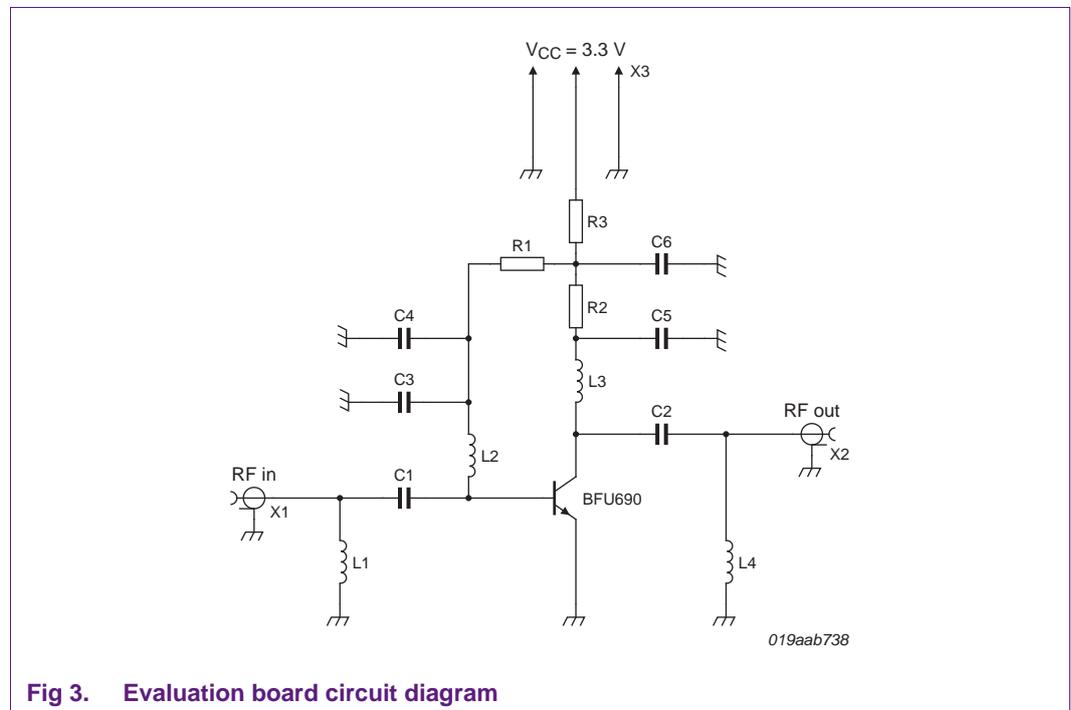


Fig 3. Evaluation board circuit diagram

3.2 Board layout

[Figure 2](#) shows the board layout with components.

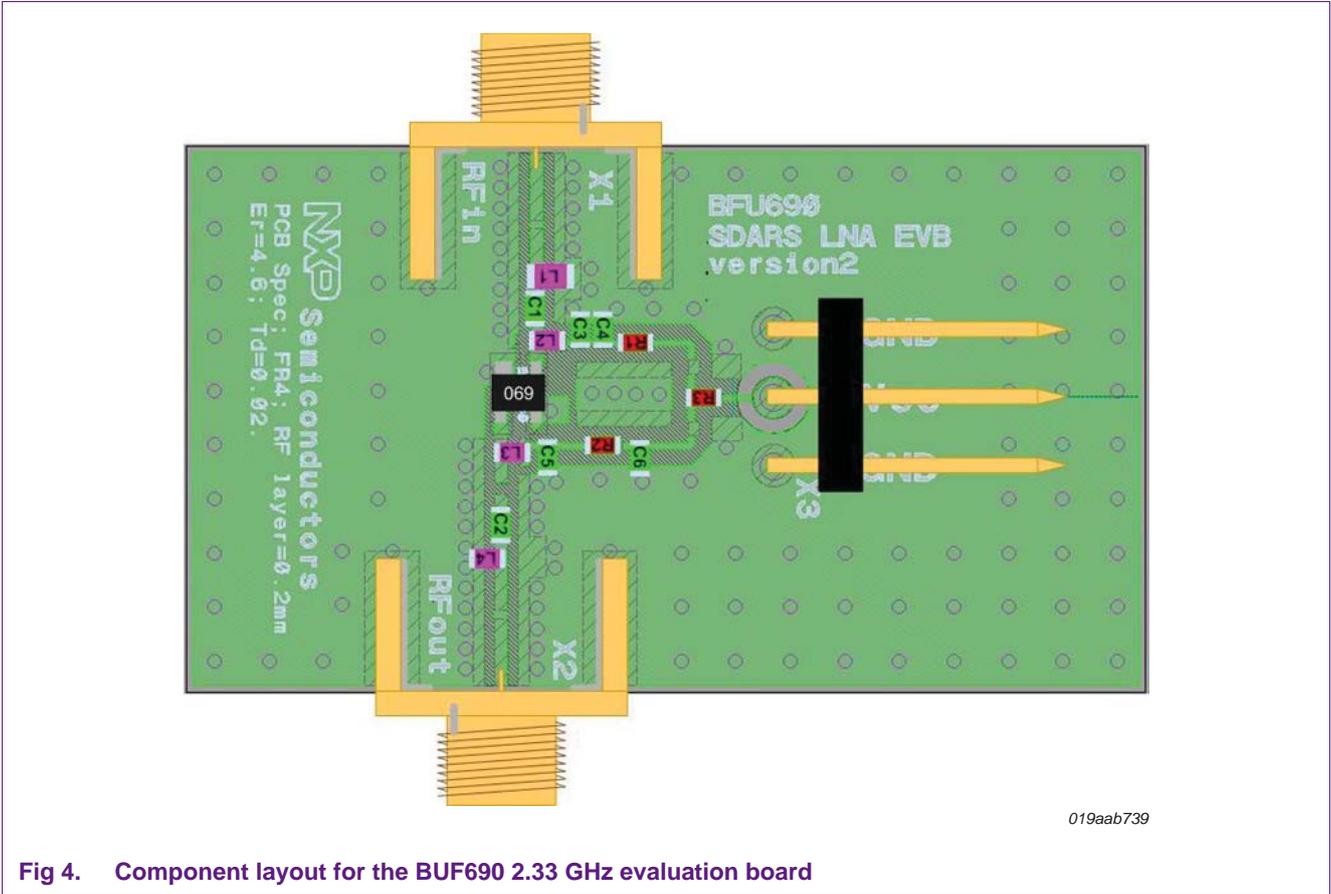


Fig 4. Component layout for the BUF690 2.33 GHz evaluation board

3.3 PCB layout

A good PCB Layout is an essential part of an RF circuit design. The EVB of the BFU690 can serve as a guideline for laying out a board using either the BFU690. Use controlled impedance lines for all high frequency inputs and outputs. Bypass supply voltage V_{CC} with decoupling capacitors, preferable located as close as possible to the device. For long bias lines it may be necessary to add decoupling capacitors along the line further away from the device. Proper grounding of the GND pin is also essential for the performance. Either connect the GND pin directly to the ground plane or through vias, or do both.

The EVB is made of FR4 material using the stack shown in [Figure 5](#)

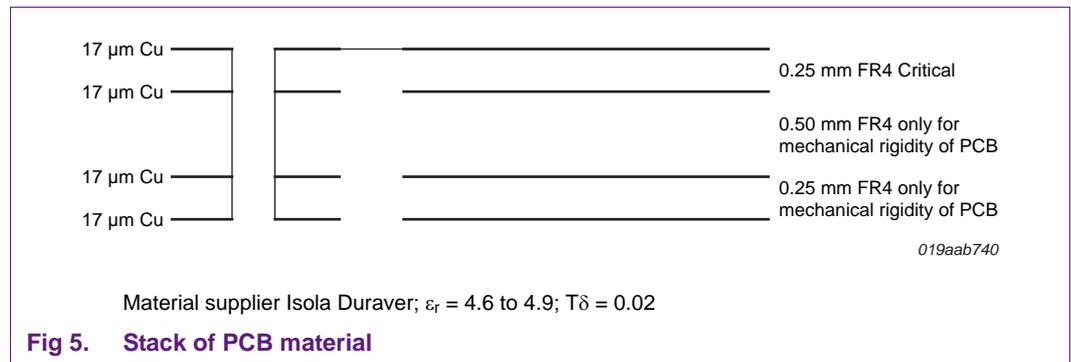


Fig 5. Stack of PCB material

3.4 Bill of materials

Table 3. Bill of materials

Component	Description	Footprint	Value	Manufacturer	Comment
C1, C2	capacitor	0402	1.8 pF	Murata GRM1555	DC blocking
C3, C5	capacitor	0402	8.2 pF	Murata GRM1555	LF decoupling
C4, C6	capacitor	0402	10 nF	Murata GRM1555	LF decoupling
L1	inductor	0402	1.6 nH	Coilcraft 0603CS; high Q, low Rs	input matching
L2	inductor	0402	12 nH	Murata/LQW15A; high Q, low Rs	input matching /DC bias
L3	inductor	0402	3.9 nH	Murata/LQW15A	input matching
L4	inductor	0402	4.1 nH	Murata/LQW15A	input matching /DC bias
R1	resistor	0402	9.1 k Ω	various	bias setting
R2	resistor	0402	22 Ω	various	stability
R3	resistor	0402	15 Ω	various	bias setting temp stability
X1, X2	SMA RF connector	-	-	Johnson, End Launch SMA 142-0701-841	RF input/ RF output
X3	DC header	-	-	Molex, PCB header, Right angle, 1 row, 3 way, Part no: 90121-0763	bias connector

4. Required equipment

In order to measure the evaluation board the following are necessary:

- DC power supply up to 60 mA at 3.3 V (up to 15 V for bias Control)
- RF signal generator capable of generating an RF signal at the 2.33 GHz operating frequency
- RF spectrum analyzer covering as a minimum the 2.33 GHz operating frequency and some of the harmonics (up to 8 GHz should be sufficient). Optional: a version with the capability of measuring noise figure is convenient
- Amp meter to measure the supply current (optional)
- NetWork analyzer for measuring gain, return loss and reverse isolation
- Noise figure analyzer.

5. Connections and setup

The BFU690, 2.33 GHz EVB is fully assembled and tested. To operate the EVB and test the device functions follow this step-by-step guide:

1. Connect the DC power supply to the V_{CC} and GND terminals and set to 3.3 V.
2. Connect the RF signal generator and the spectrum analyzer to the RF input and the RF output of the EVB respectively. Do not yet turn on the RF output of the signal generator. Set it to -30 dBm output power at 2.33 GHz and set the spectrum analyzer to 2.33 GHz center frequency with a reference level of 0 dBm.
3. Turn on the DC power supply and it should read approximately 30 mA.
4. Enable the RF output of the generator; the spectrum analyzer displays a tone of 2.33 GHz at approximately 14.7 dBm.

5. A NetWork Analyzer (NWA) can be used instead of a signal generator and spectrum analyzer in order to measure both gain and input and output return losses.
6. For noise figure evaluation use either a noise figure analyzer or a spectrum analyzer with noise option. The use of a 15 dB noise source, such as the Agilent 364B is recommended. When measuring the noise figure of the evaluation board, any kind of adaptors, cables etc, between the noise source and the EVB should be avoided, since this affects the noise performance.

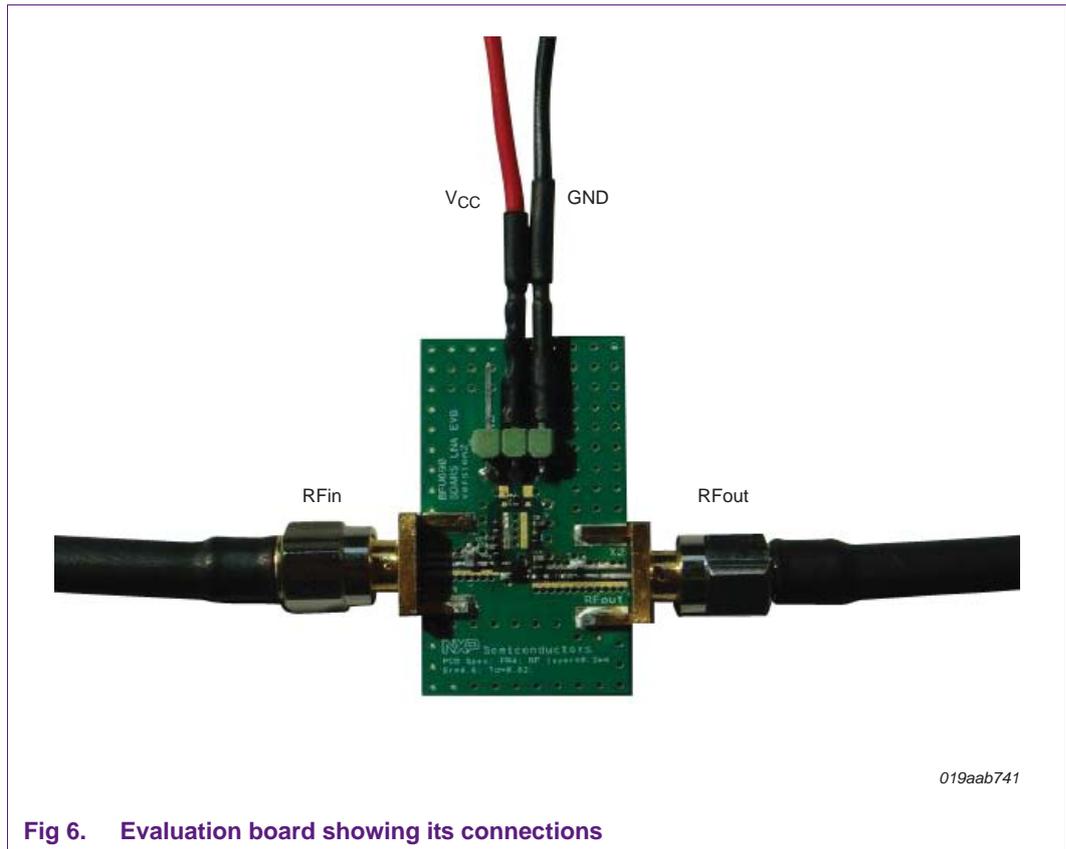


Fig 6. Evaluation board showing its connections

6. Typical EVB results

Table 4. Typical results measured on the evaluation board
T = 25 °C; f = 2.33 GHz unless otherwise specified

Symbol	Parameter	BFU690 EVB	Unit
NF	noise figure	1.47 ^[1]	dB
G _p	power gain	15.3 ^[1]	dB
IRL	input return loss	10	dB
ORL	output return loss	17	dB
$\alpha_{isol(r)}$	reverse isolation	20.7	dB
P _{i(1dB)}	input power at 1 dB gain compression	-0.48	dBm

Table 4. Typical results measured on the evaluation board ...continued
T = 25 °C; f = 2.33 GHz unless otherwise specified

Symbol	Parameter	BFU690 EVB	Unit
$P_{L(1dB)}$	output power at 1 dB gain compression	13.9	dBm
$IP3_i$	input third order intercept point	12.85	dBm
$IP3_o$	output third order intercept point	28.15	dBm

[1] The NF and gain figures are measured at the SMA connectors of the EVB, so the connector and PCB losses are not subtracted. If subtracted the NF will improve by approximately 0.1 dB.

6.1 Noise figure

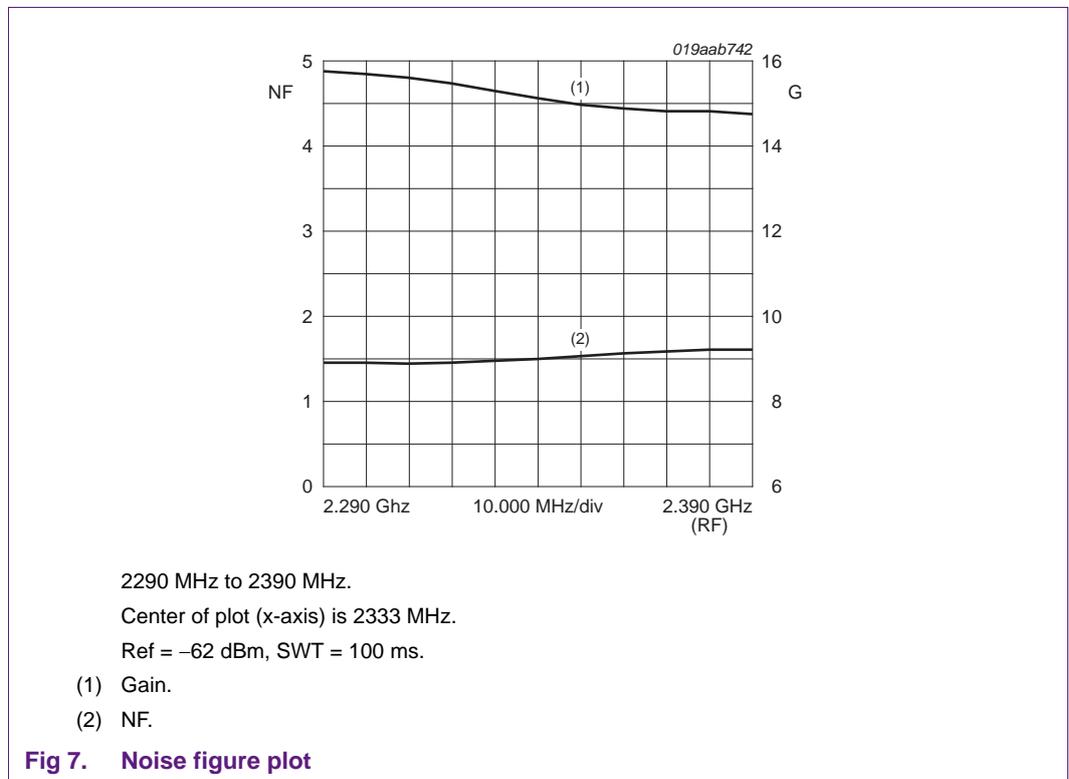


Table 5. Noise figure tabular data
 From Rohde & Schwarz FSU

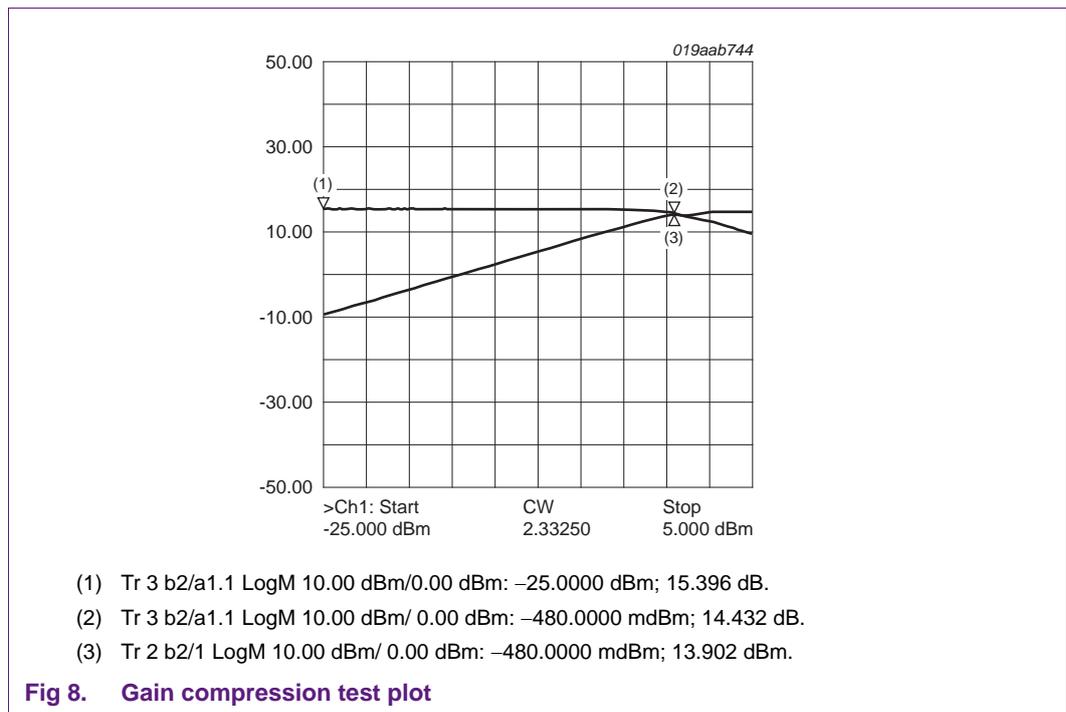
Frequency list results			
RF (GHz)	NF (dB)	Noise temp (K)	Gain (dB)
2.290	1.456	115.508	15.758
2.300	1.445	114.499	15.699
2.310	1.445	114.486	15.601
2.320	1.450	114.944	15.468
2.330	1.468	116.673	15.297
2.340	1.499	119.495	15.124

Table 5. Noise figure tabular data ...continued
From Rohde & Schwarz FSU

Frequency list results			
RF (GHz)	NF (dB)	Noise temp (K)	Gain (dB)
2.350	1.528	122.291	14.968
2.360	1.564	125.712	14.875
2.370	1.587	127.888	14.822
2.380	1.601	129.290	14.810
2.390	1.607	129.874	14.750

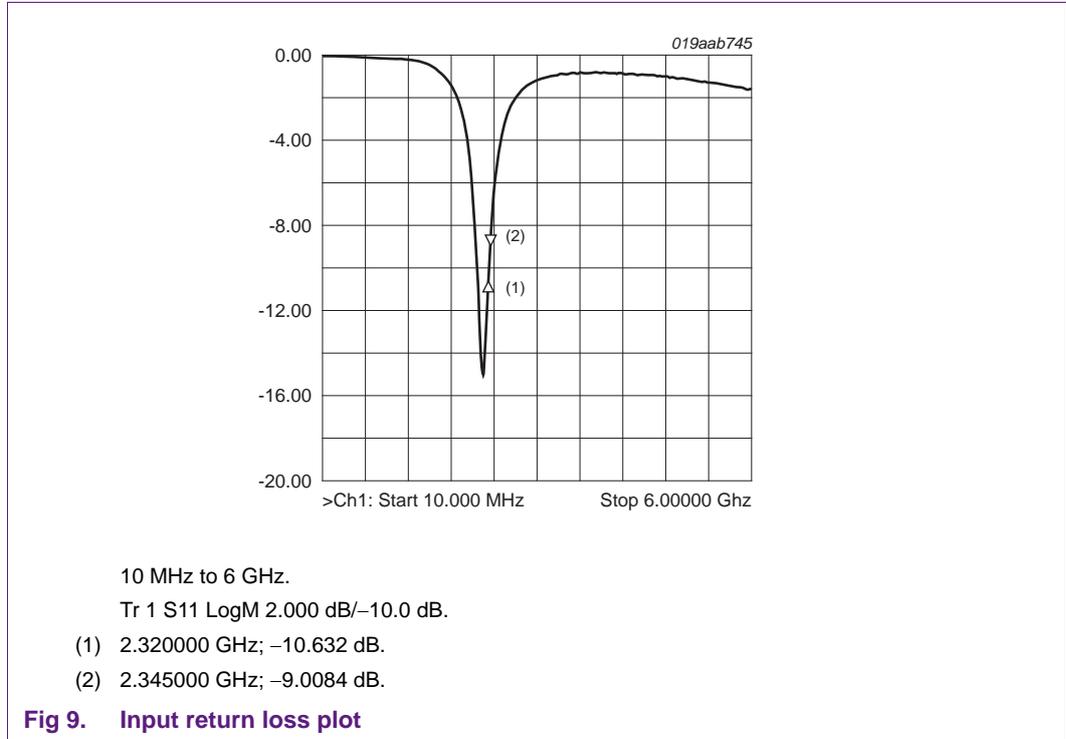
6.2 Gain compression test

The network analyzer is set to CW mode: e.g. set to a single frequency, with power sweep. Input power is swept from -25 dBm to +5 dBm at 2332.5 MHz. The amplifier reaches input 1 dB compression point ($P_{i(1dB)}$) at -0.48 dBm input power. Output $P_{L(1dB)} = -0.48 \text{ dBm} + 14.4 \text{ dB gain at } P_{L(1dB)} \text{ point} \geq +13.9 \text{ dBm}$, or 24.5 mW

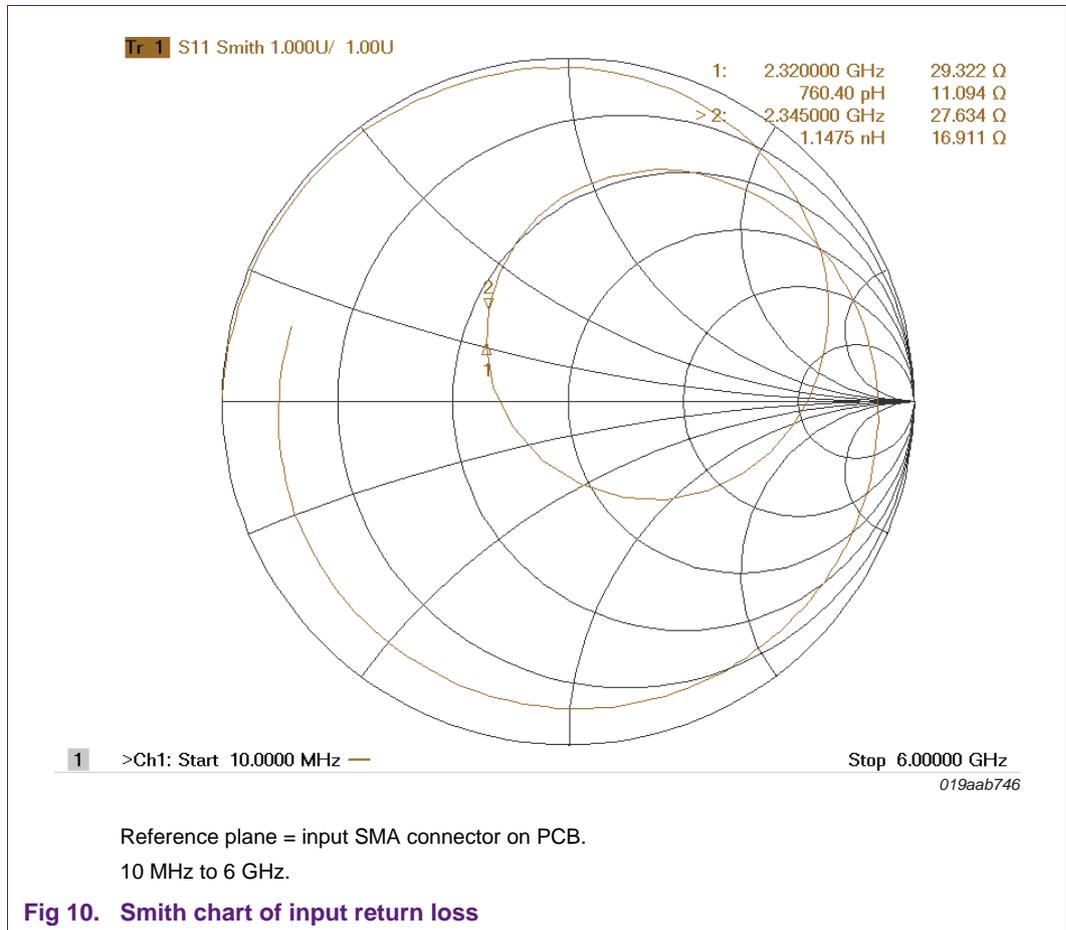


6.3 Input return losses

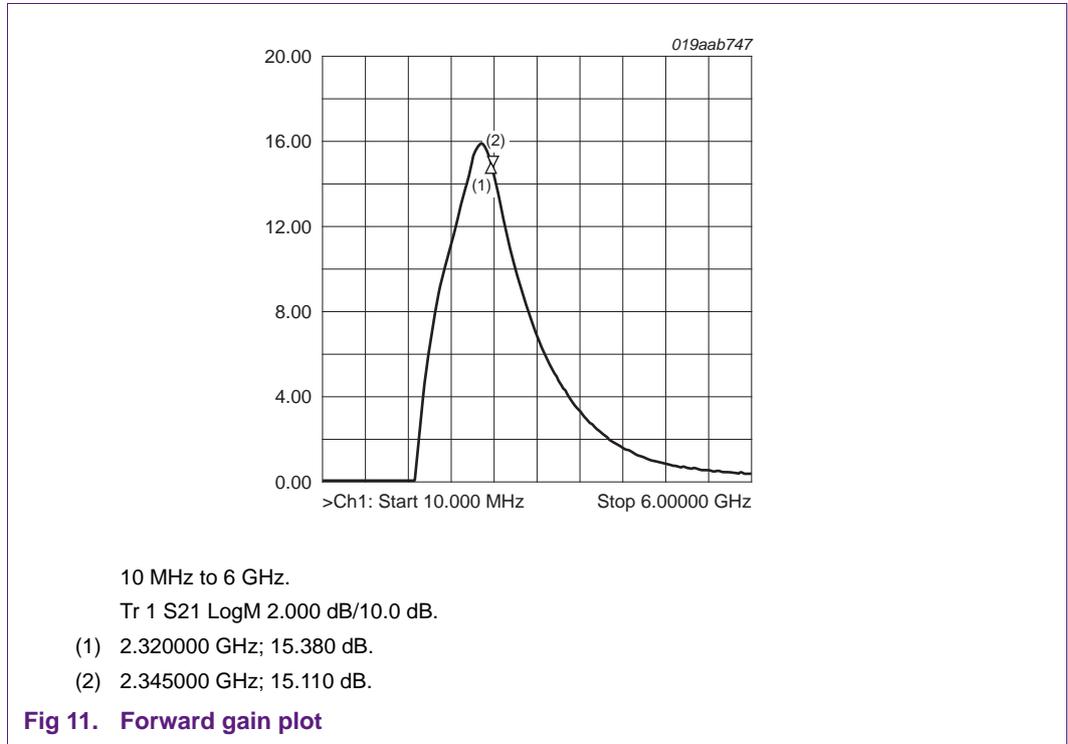
6.3.1 Log Mag



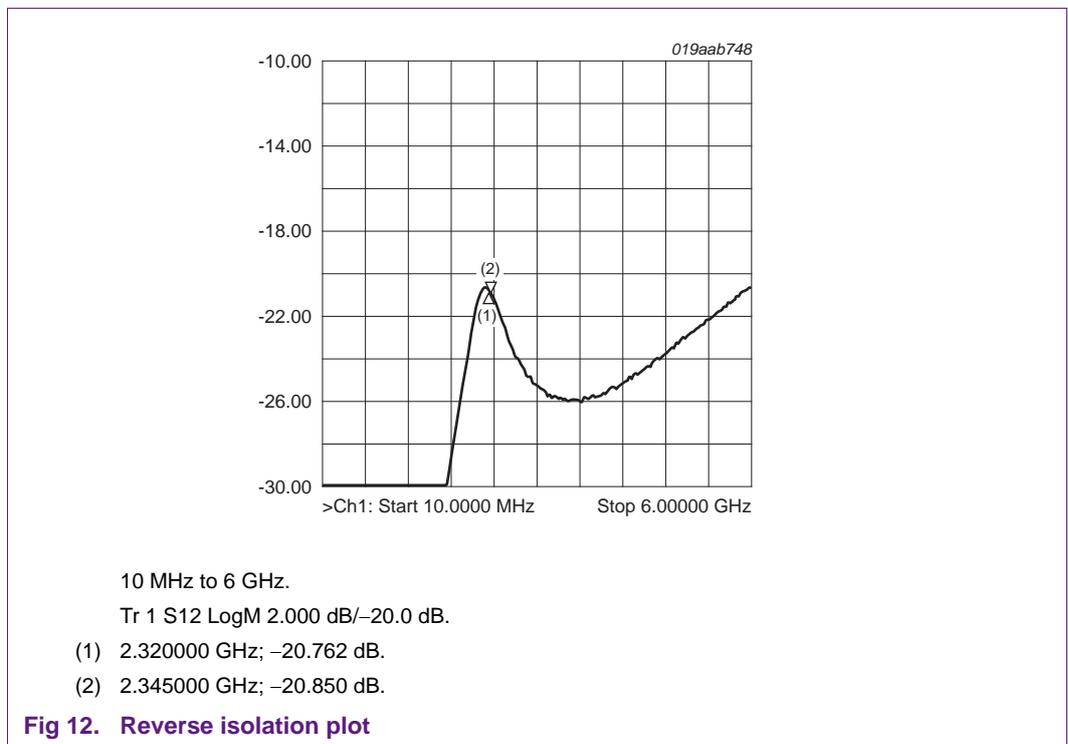
6.3.2 Smith chart



6.4 Forward gain, wide sweep

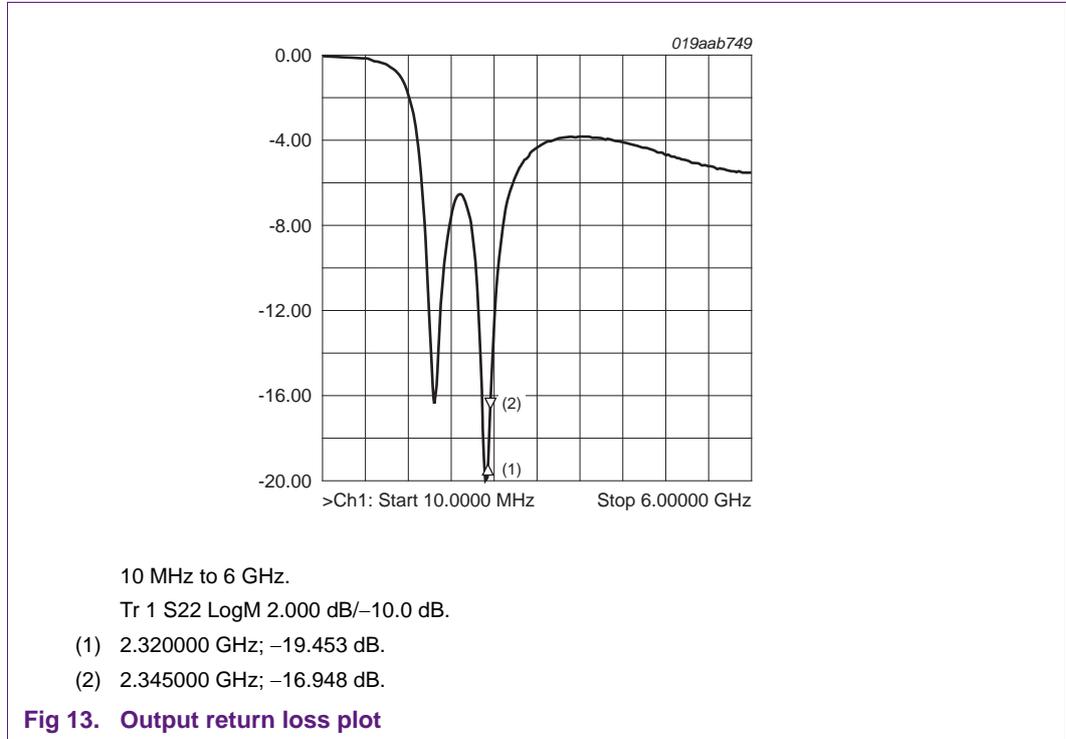


6.5 Reverse isolation

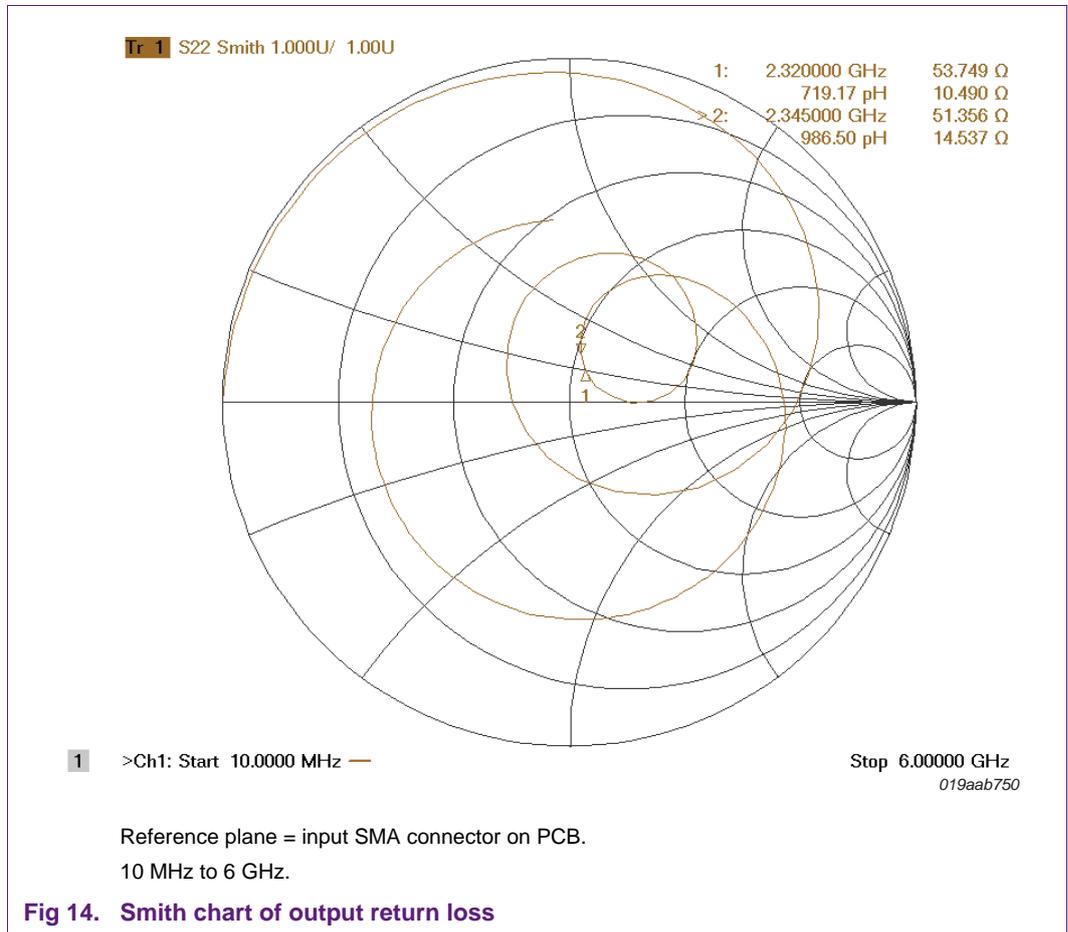


6.6 Output return losses

6.6.1 Log Mag

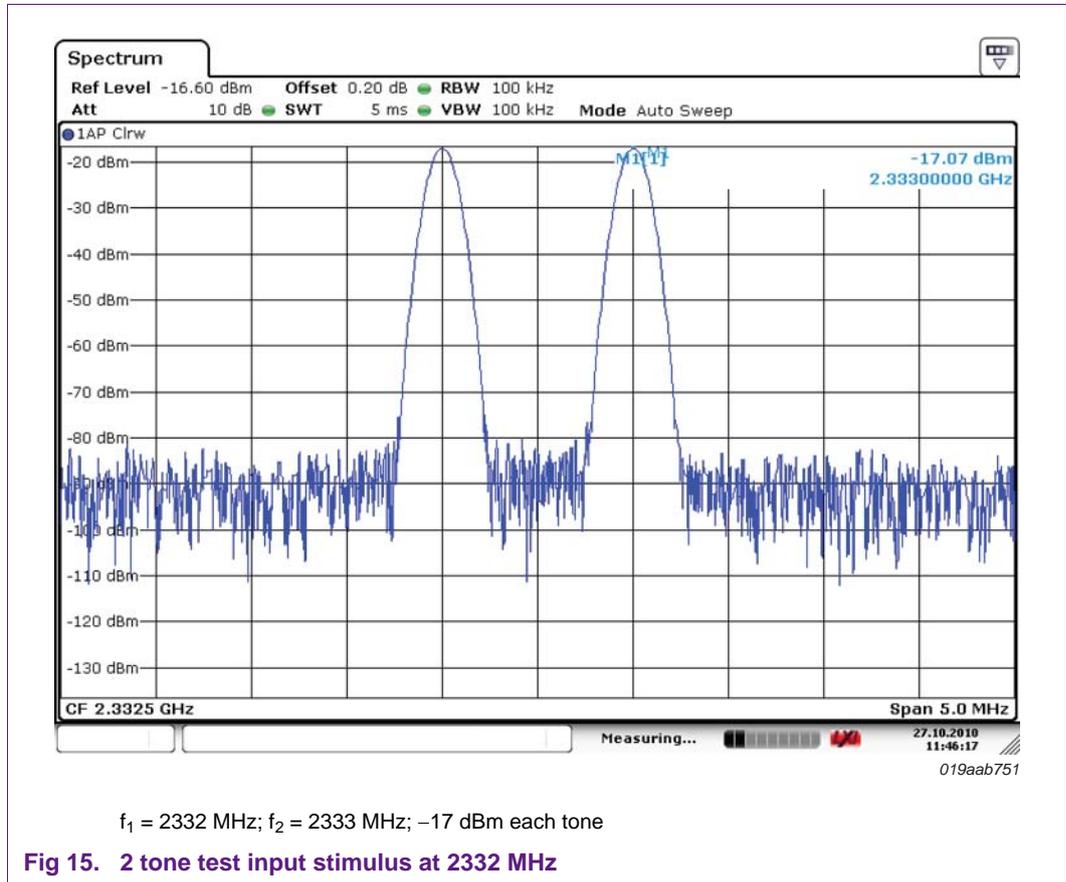


6.6.2 Smith chart

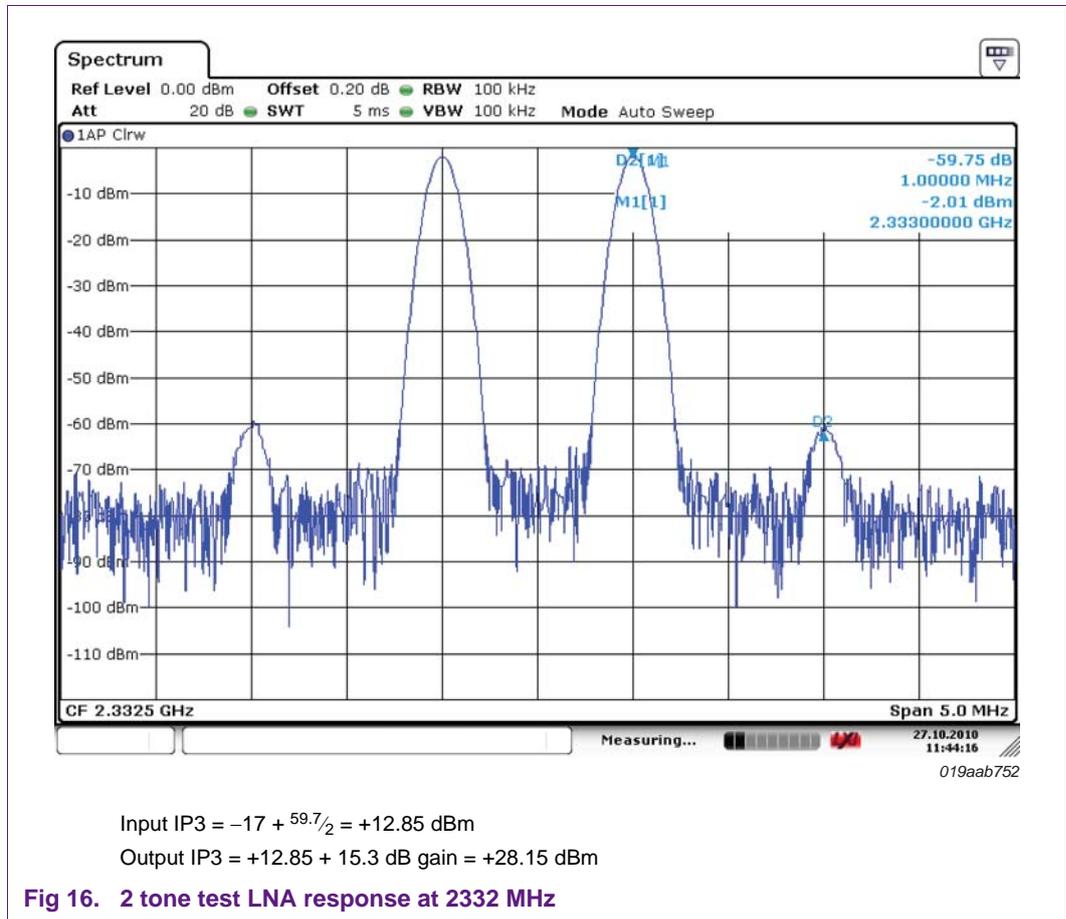


6.7 2-tone test at 2332 MHz

6.7.1 Input stimulus for amplifier 2-tone test



6.7.2 LNA response to 2-tone test



7. Abbreviations

Table 6. Abbreviations

Acronym	Description
EVB	EVALUATION BOARD
GPS	GLOBAL POSITIONING SYSTEM
LAN	LOCAL AREA NETWORK
LNA	LOW NOISE AMPLIFIER
NWA	NETWORK ANALYZER
RF	RADIO FREQUENCY
SDARS	SATELLITE DIGITAL AUDIO SERVICE

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